MOS (Metal Oxide Semiconductor) Structures

In this lecture you will learn:

- The fundamental set of equations governing the behavior of PMOS capacitors
- Accumulation, Flatband, Depletion, and Inversion Regimes
- Small signal models of the PMOS capacitor
A P-MOS (or PMOS) Capacitor

Assumptions:

1) The potential in the metal gate is $\phi_M$.
   If the gate is P+ Si then $\phi_M = \phi_D$.

2) The potential deep in the p-Si substrate is $\phi_D$.

3) The oxide (SiO$_2$) is insulating (near zero conductivity; no free electrons and holes) and is completely free of any charges.

4) There cannot be any volume charge density inside the metal gate (it is very conductive). But there can be a surface charge density on the surface of the metal gate.

5) Dielectric constants:
   $\varepsilon_{ox} = 3.9 \varepsilon_0$
   $\varepsilon_s = 11.7 \varepsilon_0$
A PMOS Capacitor in Equilibrium

Potential Plot: $\phi(x)$

We need to find the potential in equilibrium everywhere.

A PMOS Capacitor in Equilibrium: Depletion Region

Step 1: Charges Flow

Step 2: Depletion region is created in the substrate and a surface or sheet charge density on the metal gate

Negative surface charge density (C/cm²)

$Q_G = -qN_dx_{do}$

Positive depletion charge density (C/cm²)

$\rho = +qN_d$
A PMOS Capacitor in Equilibrium: Charge Densities

Charge density plot:

\[ Q_G = -qN_d x_{do} \]

Depletion region charge density (C/cm²)

Total charge per unit area in the semiconductor (C/cm²)

\[ Q_B = qN_d x_{do} \]

A PMOS Capacitor in Equilibrium: Electric Field

Electric field in the semiconductor:

\[ \frac{dE_x}{dx} = \frac{\rho}{\varepsilon_s} = \frac{qN_d}{\varepsilon_s} \]

\[ E_x(x = x_{do}) = 0 \]

\[ E_x(x) = \frac{qN_d}{\varepsilon_s} (x - x_{do}) \]

Linearity varying

\[ E_x(x = 0) = \frac{qN_d}{\varepsilon_s} x_{do} \]
Some Electrostatics
Consider an interface between media of different dielectric constants:

\[ \varepsilon_2 \vec{E}_2 - \varepsilon_1 \vec{E}_1 = Q_I = \text{Interface sheet charge density} \]

Suppose you know \( \vec{E}_1 \), can you find \( \vec{E}_2 \)???

Use the principle: The product of the dielectric constant and the normal component of the electric field on both sides of an interface are related as follows:

• Note that \( \vec{E}_1 \) is the electric field JUST to the left of the interface and \( \vec{E}_2 \) is the electric field JUST to right of the interface

A PMOS Capacitor in Equilibrium: Electric Field

Electric field in the oxide:

\[ \frac{dE_x}{dx} = \frac{\rho}{\varepsilon_{ox}} = 0 \]

\[ \Rightarrow E_x(x) = \text{constant} \]

\[ \Rightarrow E_x(x) = -\frac{qN_d x_{do}}{\varepsilon_{ox}} \]

\[ E(x = 0^-) = E(x = 0^+) \]

\[ E(x) = -\frac{qN_d x_{do}}{\varepsilon_s} = E_{ox} \]

\[ \Rightarrow E(x = 0^-) = -\frac{qN_d x_{do}}{\varepsilon_{ox}} = E_{ox} \]
A PMOS Capacitor in Equilibrium: Potential

Potential in the semiconductor:
\[ \frac{d\phi(x)}{dx} = -E_x(x) = -\frac{qN_D}{\varepsilon_s} (x - x_{do}) \]
\[ \{ \phi(x = x_{do}) = \phi_n \] 
\[ \phi(x) = \phi_n - \frac{qN_D}{2\varepsilon_s} (x - x_{do})^2 \]

Potential in the oxide:
\[ \frac{d\phi(x)}{dx} = -E_x(x) = \frac{qN_D x_{do}}{\varepsilon_{ox}} \]
\[ \{ \phi(x = 0) = \phi_n - \frac{qN_D x_{do}^2}{2\varepsilon_s} \] 
\[ \phi(x) = \phi_n - \frac{qN_D x_{do}^2}{2\varepsilon_s} + \frac{qN_D x_{do}}{\varepsilon_{ox}} x \]
A PMOS Capacitor in Equilibrium: Potential

Potential drop in the oxide

Potential drop in the semiconductor

Oxide capacitance (per unit area)

Potential drop in the semiconductor

Oxide capacitance (per unit area)

Potential drop in the oxide

\[
\phi(x = -t_{ox}) = \phi_n - \frac{qN_d x_{do}^2}{2\varepsilon_s} - \frac{qN_d x_{do} t_{ox}}{\varepsilon_{ox}} = \phi_M
\]

Therefore:

\[
x_{do} = \frac{\varepsilon_s}{C_{ox}} + \left( \frac{\varepsilon_s}{C_{ox}} \right)^2 \left( \frac{qN_d x_{do}}{2\varepsilon_s} \right) (-\phi_B)
\]

\[
\phi_B = \phi_M - \phi_n
\]

\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}
\]

\[
E_{ox} = -\frac{qN_d x_{do}}{\varepsilon_{ox}}
\]

\[
\phi_B = \phi_M - \phi_n
\]

\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}
\]
A Biased PMOS Capacitor: $V_{GB} > 0$

All of the applied bias falls across the depletion region and the oxide

$$-\phi_B - V_{GB} = \frac{qN_d x_d}{C_{ox}} + \frac{qN_d x_d^2}{2\varepsilon_s}$$

Potential drop in the oxide

Potential drop in the semiconductor

The depletion region shrinks and the oxide field also decreases for $V_{GB} > 0$

$$x_d = -\frac{\varepsilon_s}{C_{ox}} + \left(\frac{\varepsilon_s}{C_{ox}}\right)^2 + \frac{2\varepsilon_s}{qN_d}(-\phi_B - V_{GB})$$

$$E_{ox} = -\frac{qN_d x_d}{\varepsilon_{ox}}$$
A Biased PMOS Capacitor: Flatband Condition

When \( V_{GB} \) is sufficiently positive, the depletion region thickness shrinks to zero. This value of \( V_{GB} \) is called the flatband voltage \( V_{FB} \).

Potential in flatband condition:

Flatband voltage:

\[
x_d = -\frac{\varepsilon_s}{C_{ox}} + \left( \frac{\varepsilon_s}{C_{ox}} \right)^2 + \frac{2\varepsilon_s}{qN_d} (\phi_B - V_{FB}) = 0
\]

\[
\Rightarrow V_{FB} = -\phi_B = -(\phi_M - \phi_n)
\]

A Biased PMOS Capacitor: Accumulation (\( V_{GB} > V_{FB} \))

Potential:

Charge density:

\[
Q_G = C_{ox} (V_{GB} - V_{FB})
\]

\[
Q_N = -C_{ox} (V_{GB} - V_{FB})
\]
A Biased PMOS Capacitor: Depletion ($V_{GB} < V_{FB}$)

\[ V_{GB} - V_{FB} = \frac{qN_d x_d}{C_{ox}} - \frac{qN_d x_d^2}{2 \varepsilon_s} \]

\[ \Rightarrow V_{GB} - V_{FB} = \phi_s - \phi_n - \frac{\sqrt{2 \varepsilon_s qN_d (\phi_s + \phi_n)}}{C_{ox}} \]

Potential drop in the oxide
Potential drop in the semiconductor

The depletion region widens and the oxide field also increases for $V_{GB} < V_{FB}$.
A Biased PMOS Capacitor: Hole Density

- As $V_{GB}$ is decreased, $\phi_S$ also decreases.
- The hole density in the semiconductor depends on the potential as:

\[
\rho(x) = n_i e \cdot \frac{q(-\phi_S + \phi_n)}{K_T} = N_d e \cdot \frac{q(-\phi_S + \phi_n)}{K_T}
\]

Hole density is the largest right at the surface of the semiconductor where the potential is the lowest:

\[
\rho(x = 0) = N_d e \cdot \frac{q(-\phi_S - \phi_n)}{K_T}
\]

A Biased PMOS Capacitor: Threshold Condition

- When $V_{GB}$ is decreased and the surface potential $\phi_S$ reaches $-\phi_n$, the positive hole charge density at the surface becomes comparable to the positive charge density in the depletion region and cannot be ignored.
- The gate voltage at which $\phi_S$ equals $-\phi_n$ is called the threshold voltage $V_{TP}$:

\[
V_{TP} - V_{FB} = -2\phi_n - \frac{\sqrt{2\varepsilon_S qN_d (2\phi_n)}}{C_{ox}}
\]
A Biased PMOS Capacitor: Inversion \((V_{GB} < V_{TP})\)

- When the gate voltage \(V_{GB}\) is decreased below \(V_{TP}\) the hole density right at the surface increases (exponentially with the decrease in the surface potential \(\phi_S\)).
- This surface hole density is called the inversion layer (assumed to be of zero thickness in this course).

Inversion layer charge (due to holes) on the semiconductor surface

\[
-Q_p = \text{Inversion layer charge density (C/cm}^2\text{)}
\]

\[
Q_G = -qN_d x_d - Q_p
\]

A Biased PMOS Capacitor: Inversion \((V_{GB} < V_{TP})\)

- When the gate voltage \(V_{GB}\) is decreased below \(V_{TP}\) the inversion layer charge increases so rapidly that the extra applied potential drops entirely across the oxide, and the surface potential \(\phi_S\) remains close to \(-\phi_n\).
- Consequently, the depletion region thickness (and the depletion region charge) does not increase when the gate voltage \(V_{GB}\) is decreased below \(V_{TP}\).
A Biased NMOS Capacitor: Inversion ($V_{GB} < V_{TP}$)

How to calculate the inversion layer charge $Q_p$ when $V_{GB} < V_{TP}$?

Start from: $V_{FB} - V_{GB} = V_{ox} + V_S$

$$= -E_{ox} t_{ox} + \frac{qN_d x_{d,max}^2}{2\varepsilon_s}$$

By Gauss' law: $-\varepsilon_{ox} E_{ox} = Q_p + qN_d x_{d,max}$

Therefore:

$$V_{FB} - V_{GB} = \frac{Q_p}{C_{ox}} + \frac{qN_d x_{d,max}^2}{2\varepsilon_s}$$

$$\Rightarrow V_{GB} = -\frac{Q_p}{C_{ox}} + V_{TP}$$

$$\Rightarrow Q_p = -C_{ox} (V_{GB} - V_{TP})$$

A Biased PMOS Capacitor: Summary of Different Regimes

Flatband ($V_{GB} = V_{FB}$):

No depletion region in the semiconductor and no accumulation charge

Accumulation ($V_{GB} > V_{FB}$):

No depletion region in the semiconductor but majority carrier accumulation charge on the surface of the semiconductor

Depletion ($V_{TP} < V_{GB} < V_{FB}$):

Depletion region in the semiconductor but no majority carrier accumulation charge or minority carrier inversion charge on the surface of the semiconductor

Inversion ($V_{GB} < V_{TP}$):

Depletion region in the semiconductor and minority carrier inversion charge on the surface of the semiconductor
A Biased PMOS Capacitor: Charges

Depletion Region Charge (C/cm²)

\[ Q_B = qN_d x_d^{max} = \sqrt{2\varepsilon_x N_d (2\Phi_H)} \]

\[ Q_B = qN_d x_d = qN_d \left\{ -\frac{\varepsilon_x}{C_{ox}} + \left( \frac{\varepsilon_x}{C_{ox}} \right)^2 \right\} \left( \frac{2\varepsilon_x}{qN_d} (V_{GB} - V_F) \right) \]

Inversion Layer Charge (C/cm²)

\[ Q_P = -C_{ox} (V_{GB} - V_T) \]

Accumulation Layer Charge (C/cm²)

\[ Q_N = -C_{ox} (V_{GB} - V_F) \]

Gate Charge (C/cm²)

\[ Q_G = -Q_P - Q_N - Q_B \]
The Small Signal Capacitance of a PMOS Capacitor

• The small signal capacitance (per unit area) of the MOS capacitor is defined as:

\[
C = \frac{dQ_G}{dV_{GB}}
\]

where \( Q_G \) is the charge density (units: C/cm²) on the gate.

(1) Accumulation (\( V_{GB} > V_{FB} \)):

\[
Q_G = C_{ox} (V_{GB} - V_{FB})
\]

\( \Rightarrow C = C_{ox} \)

(2) Depletion (\( V_{TP} < V_{GB} < V_{FB} \)):

\[
Q_G = -qN_d x_d
\]

\[
C = \frac{dQ_G}{dV_{GB}} = -qN_d \frac{dx_d}{dV_{GB}}
\]

Differentiate the equation (derived earlier):

\[
\frac{qN_d x_d^2}{2 \varepsilon_s} + \frac{qN_d x_d}{C_{ox}} = -V_{GB} + V_{FB}
\]

To get:

\[
\left[ \frac{x_d}{\varepsilon_s} + \frac{1}{C_{ox}} \right] qN_d \ dx_d = -dV_{GB}
\]

Define:

\[
C_b = \frac{\varepsilon_s}{x_d}
\]

Finally:

\[
\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_b}
\]
The Small Signal Capacitance of a PMOS Capacitor

(3) Inversion ($V_{GB} < V_{TP}$):

\[
Q_G = -qN_d x_{d\text{max}} - Q_P
\]

\[
C = \frac{dQ_G}{dV_{GB}} = -\frac{dQ_P}{dV_{GB}} = C_{ox}
\]

\[
Q_P = -C_{ox} (V_{GB} - V_{TP})
\]

$x_{d\text{max}}$ does not change with $V_{GB}$ in inversion.

The Small Signal Capacitance of a PMOS Capacitor

Gate Charge

(C/cm²)

\[
C = \frac{dQ_G}{dV_{GB}}
\]

Q

C

$V_{TP}$

$V_{FB}$

V

$V_{GB}$

$C_{ox}$

Inversion

Accumulation

Depletion
• In the presence of an inversion layer, the additional contacts allow one to directly change the potential of the inversion layer channel w.r.t. to the bulk (substrate).

We had said that the surface potential $\psi_s$ remains fixed at $-\psi_n$ when $V_{GB}$ is decreased below $V_{TF}$

But with a non-zero $V_{CB}$, the surface potential $\psi_s$ in inversion can be changed to $(-\psi_n + V_{CB})$

The new value of the depletion region width is:

$$\psi_s - \psi_n = -\frac{qN_d x_d^2}{2\varepsilon_s} \Rightarrow -2\psi_n + V_{CB} = -\frac{qN_d x_{d,max}^2}{2\varepsilon_s}$$

Question: How do we now find the inversion layer charge $Q_P$ when $V_{CB}$ is not zero?
A Biased NMOS Capacitor: Inversion with $V_{CB} \neq 0$

How to calculate the inversion layer charge $Q_p$? Same way as before……..

Start from: $V_{FB} - V_{GB} = V_{oX} + V_S$

$$V_S = \frac{qN_d x_{d\text{max}}^2}{2\varepsilon_s}$$

By Gauss’ law: $-\varepsilon_{oX} E_{oX} = Q_p + qN_d x_{d\text{max}}$

Therefore: $V_{FB} - V_{GB} = \frac{Q_p}{C_{oX}} + \frac{qN_d x_{d\text{max}}}{C_{oX}} + \frac{qN_d x_{d\text{max}}^2}{2\varepsilon_s}$

$$V_{GB} = -\frac{Q_p}{C_{oX}} + V_{FB} - \frac{qN_d x_{d\text{max}}}{C_{oX}} - \frac{qN_d x_{d\text{max}}^2}{2\varepsilon_s}$$

$V_{TP} = V_{FB} - \frac{qN_d x_{d\text{max}}}{C_{oX}} - \frac{qN_d x_{d\text{max}}^2}{2\varepsilon_s}$

$$= V_{FB} - 2\Phi_n + V_{CB} - \frac{2\varepsilon_S q N_d (2\Phi_n - V_{CB})}{C_{oX}}$$

$\Rightarrow Q_p = -C_{oX} (V_{GB} - V_{TP})$  

Same as before but now $V_{TP}$ depends on $V_{CB}$
PMOS Capacitor: Effect of $V_{CB}$ ($V_{GB} < V_{TP}$)

- $V_{CB} < 0$
  - Inversion charge decreases
  - Depletion region expands

- $V_{CB} > 0$
  - Inversion charge increases
  - Depletion region shrinks