In this lecture you will learn:

- Circuits for wireless communications
- Signal multipliers and mixers
- Single-balanced and double-balanced mixers
- CMOS RF Oscillators
- Analog to digital converters
- Digital to analog converters

Signal Transmission in Wireless Communications

- Sound waves
- Electrical analog signal
- Low noise Amplifier (LNA)
- Digital Output
- Power amplifier (PA)
- Antenna
- E&M Radiation
- Filter
- Electrical analog signal
- Constellation size: $2^M$
- Information in bits per point in the constellation: $M$
Signal Reception in Wireless Communications

Sound waves | Electrical analog signal | DAC
|---|---|---

Digital input | N-bits

PA Filter

Antenna

LNA

Filter

Mixer or demodulator

Digital decoder

QAM signal constellation

RF Mixer or Modulator/Demodulator

QAM RF signals

\[ X_1(t) \cos(\omega_{LO}t) + X_2(t) \sin(\omega_{LO}t) = A(t) \cos(\omega_{LO}t + \phi(t)) \]

\[ X_1(t) \cos(\omega_{LO}t) + X_2(t) \sin(\omega_{LO}t) \]

\[ \cos(\omega_{LO}t) \cos(\omega_{LO}t) = \frac{1}{2} \cos(2\omega_{LO}t) \]

\[ \sin(\omega_{LO}t) \sin(\omega_{LO}t) = \frac{1}{2} \cos(2\omega_{LO}t) \]

\[ \cos(\omega_{LO}t) \sin(\omega_{LO}t) = \frac{1}{2} \sin(2\omega_{LO}t) \]
Signal Mixers

Mixer Function:
\[ X_1(t) = v_{RF} \cos(\omega_{RF}t) \]
\[ v_{LO} \cos(\omega_{LO}t) \]
\[ A_{RF}v_{LO} \cos(\omega_{RF}t) \cos(\omega_{LO}t) \]
\[ \frac{A}{2}v_{RF}v_{LO} \left[ \cos\left((\omega_{LO} + \omega_{RF})t\right) + \cos\left((\omega_{LO} - \omega_{RF})t\right) \right] \]

\[ \omega_{LO} \gg \omega_{RF} \]

Mixer Conversion Gain:
Conversion gain = \( G_c = \frac{A}{2} \frac{v_{RF}v_{LO}}{v_{RF}} = \frac{A}{2}v_{LO} \)

Need a strong LO signal to obtain a good conversion gain

Need nonlinear components to realize voltage mixers and/or multipliers

FET Signal Mixer: Square Law Mixer

At resonance the impedance of the LC tank is ideally infinite

Forget the output conductance for a moment, then:
\[ i_D = \frac{k_n}{2} \left[ V_B + v_{RF} \cos(\omega_{RF}t) - v_{LO} \cos(\omega_{LO}t) - V_T \right]^2 \]
\[ = \frac{k_n}{2} \left[ V_B - V_T \right]^2 + \frac{k_n}{2} \left[ v_{RF} \cos(\omega_{RF}t) - v_{LO} \cos(\omega_{LO}t) \right]^2 \]
\[ + k_n \left[ V_B - V_T \right] \left[ v_{RF} \cos(\omega_{RF}t) - v_{LO} \cos(\omega_{LO}t) \right] \]
At resonance the impedance of the LC tank is ideally infinite.

Forget the output conductance for a moment, then:

\[
i_D = \frac{k_m}{2} [V_B - V_{TN}]^2 + \frac{k_n}{4} [v_{RF}^2 + v_{LO}^2] + \frac{k_n}{4} [v_{RF}^2 \cos(2\omega_{RF}t) + v_{LO}^2 \cos(2\omega_{LO}t)]
- k_n v_{RFLO} \cos(\omega_{RF}t) \cos(\omega_{LO}t)
+ k_n [V_B - V_{TN}] v_{RF} \cos(\omega_{RF}t) - v_{LO} \cos(\omega_{LO}t)
\]
The dominant signal components at the output near the frequency $\omega_{LO}$ are:

$$V_{OUT}(t) = \frac{k_n}{2} v_{RF} v_{LO} \Re \left( \frac{1}{\frac{1}{LC} \cdot \omega^2 + j \frac{1}{r_C} \omega} \right) e^{j \omega t}$$

$$+ \frac{k_n}{2} v_{RF} v_{LO} \Re \left( \frac{1}{\frac{1}{LC} \cdot \omega^2 + j \frac{1}{r_C} \omega} \right) e^{j \omega t}$$

$$+ g_m v_{GS} v_{RF} \Re \left( \frac{1}{\frac{1}{LC} \cdot \omega^2 + j \frac{1}{r_C} \omega} \right) e^{j \omega t}$$

Conversion gain = $G_C$

$$G_C = \frac{k_n}{2} v_{RF} v_{LO} r_o$$

Provided:

$$\frac{2 \sqrt{2} I_{BIAS} k_n}{k_n} \gg (V_{I1} - V_{I2})$$

$$V_{Od} = V_{O1} - V_{O2} = -Rk_n \left( \frac{V_{I1} - V_{I2}}{2} \right)$$

Assume small
A single-balanced mixer:

\[ V_{od} = V_{o1} - V_{o2} = -Rk_n \frac{(V_{i1} - V_{i2})^2}{2} \sqrt{4I_{BIAS}^2} \]

\[ I_{BIAS} = \frac{K_n}{2} (U_i - V_{TN})^2 \]

But still not quite what one would want………

i) The input voltage \( U_i \) is not differential………

ii) The two input voltages being multiplied don’t appear symmetrically in the final answer

iii) There is an additional term proportional only to \( V_{i1} - V_{i2} \) in the output
FET Signal Mixer/Multiplier: Single-Balanced Mixer

\[
V_{\text{OUT}}(t) = \frac{k_nK}{2}(r_{\text{on}} \parallel r_{\text{op}}) V_{\text{RF}} V_{\text{LO}} \cos(\omega_{\text{RF}} t) \cos(\omega_{\text{LO}} t) - \frac{k_nK}{2}(r_{\text{on}} \parallel r_{\text{op}})(V_{\text{BIAS}} - V_{\text{TIN}}) V_{\text{LO}} \cos(\omega_{\text{LO}} t)
\]

Conversion gain = \( G_C \)

\[
G_C = \frac{1}{2} \frac{k_nK_v}{2} V_{\text{RF}} V_{\text{LO}} \left( r_{\text{on}} \parallel r_{\text{op}} \right)
\]

FET Signal Mixer/Multiplier: A Double-Balanced Mixer

A cross-coupled double-balanced differential pair

\[
I_{\text{Da}} + I_{\text{Db}} = I_{L1}
\]
\[
I_{\text{Dc}} + I_{\text{Dd}} = I_{L2}
\]
\[
I_{L1} + I_{L2} = I_{\text{BIAS}}
\]

Not good
A cross-coupled double-balanced differential pair

\[ V_{id} = V_{i1} - V_{i2} \]

\[ V_{11} = (V_{i1} - V_{i2})(U_{i1} - U_{i2}) \]

\[ U_{id} = U_{i1} - U_{i2} \]

Exactly what one would want!  

Product terms

FET Signal Mixer/Multiplier: A Double-Balanced Mixer

\[ I_{D1} + I_{D2} = I_{L1} \]

\[ I_{D1} + I_{Dd} = I_{L2} \]

\[ I_{L1} + I_{L2} = I_{BIAS} \]

\[ I_{D1} = \frac{k_n}{2} [V_{GS1} - V_{TN}]^2 \left[ \frac{4}{4} \right] \]

\[ I_{D2} = \frac{k_n}{2} [V_{GS2} - V_{TN}]^2 \left[ \frac{4}{4} \right] \]

\[ I_{Dd} = \frac{k_n}{2} [V_{GSd} - V_{TN}]^2 \left[ \frac{4}{4} \right] \]

\[ I_{Dv} = \frac{k_n}{2} [V_{GSv} - V_{TN}]^2 \left[ \frac{4}{4} \right] \]

\[ V_{OD} = V_{O1} - V_{O2} = -(I_{D1} + I_{D2})R + (I_{D1} + I_{Dd})R \]

\[ = -R k_n \left( \frac{V_{i1} - V_{i2}}{2} \right)^2 \]

\[ = -R k_n \left( \frac{V_{i1} - V_{i2}}{2} \right)^2 \]

Oscillators: Electronic, Photonic, and Spintronic

Photonic Oscillators (Lasers)  
(2 THz – 2000 THz)

CMOS THz Oscillators  
(Cornell)  
(100 GHz – 500 GHz)

Plasmonic Nanopatch Spasers  
(Cornell, UCB)

Fiber lasers (Cornell)

Electronic Spins Oscillators (Cornell)  
(100 MHz – 2000 GHz)

Semiconductor lasers  
(Cornell)

Electro Optic Modulator (STO)  
100 nm
Consider the following circuit with positive feedback:

\[ v_{in}(t) = 0 \]

\[ v_{out}(t) \]

In steady state operation (when one can use phasors):

\[ v_{out}(\omega) = \frac{A(\omega)}{1 - KA(\omega)} v_{in}(\omega) \]

\[ [1 - KA(\omega)] v_{out}(\omega) = A(\omega) v_{in}(\omega) \]

Loop gain: \( A(\omega)K \)

One can have a non-zero output at frequency \( \omega \) with no input, if at that frequency:

\[ [1 - KA(\omega)] v_{out}(\omega) = 0 \]

\[ \Rightarrow 1 - KA(\omega) = 0 \]

\[ \Rightarrow A(\omega)K = 1 \]

\[ \Rightarrow |A(\omega)K| = 1 \quad \text{and} \quad \angle[A(\omega)K] = 2\pi n \quad \{ n = 0, 1, 2, \ldots \} \]

For steady state oscillation, the loop gain must equal unity.

The unity loop gain condition \( A(\omega)K = 1 \) could be met (or almost met) at many different frequencies at the same time!

Add a bandwidth limiting element in the loop – a narrow bandpass filter:

Now the condition for steady state oscillation at the frequency \( \omega \) becomes:

\[ A(\omega)F(\omega)K = 1 \quad \text{Will favor oscillation at frequency } \omega_b \]
Now the condition for steady state oscillation at the frequency $\omega_o$ is: $A(\omega_o)F(\omega_o)K = 1$

But is the oscillation going to be stable?

Q: What if the loop gain is slightly larger than unity: $|A(\omega_o)F(\omega_o)K| > 1$

The oscillations will build up to infinity (phasor analysis not valid anymore because there is no steady state)

Q: What if the loop gain is slightly smaller than unity: $|A(\omega_o)F(\omega_o)K| < 1$

The oscillations might never build up

What if the gain $A(\omega)$ is a non-linear decreasing function of the input signal power:

$u_{in}(\omega) \rightarrow A(\omega) \rightarrow u_{out}(\omega)$

Then the condition for stable steady state oscillation becomes:

$A(\omega_o)F(\omega_o)K = 1$

$\Rightarrow \frac{a(\omega_o)}{1 + \frac{|u_{in}(\omega)|^2}{\alpha^2}} F(\omega_o)K = 1$

Stable provided: $|a(\omega_o)F(\omega_o)K| > 1$

The signal looping around in the oscillator will adjust its magnitude automatically such that the unity gain condition is met.....!!!
Electrical Oscillators: A Phenomenological Introduction

\[
A(\omega) \xrightarrow{F(\omega)} v_{out}(t)
\]

Conditions necessary (but not sufficient) for stable steady state oscillations:

1) The complex loop gain must equal unity

2) There must be a bandwidth limiting element (or a filter) in the loop

3) The magnitude of the loop gain must be a decreasing function of the loop signal power (this is called gain saturation)

FET Electrical Oscillators: Colpitts Oscillator

A common gate FET stage connected in a positive feedback loop used can be used to realize an oscillator
Gain Saturation in FETs

As the input small signal increases in strength, the gain experienced by it will decrease.

Colpitts Oscillator

A common gate FET stage connected in a positive feedback loop can be used to realize an oscillator.
Assume the capacitors internal to the FET, $C_{gs}$ and $C_{gd}$, are open at the frequencies of interest.

KCL at (1):
\[
\frac{V_{out}(\omega)}{j\omega + r_o} \quad - \quad \frac{V_{out}(\omega) - V_s(\omega)}{r_o} \quad + \quad j\omega C_1 [V_{out}(\omega) - V_s(\omega)] = 0
\]

KCL at (2):
\[-j\omega C_2 V_s(\omega) - g_m V_s(\omega) + \frac{V_{out}(\omega) - V_s(\omega)}{r_o} + j\omega C_1 [V_{out}(\omega) - V_s(\omega)] = 0\]

These give:
\[\Rightarrow \frac{V_{out}(\omega)}{j\omega + r_o} = -j\omega C_2 V_s(\omega)\]

Compare with:
\[[1 - KA(\omega)] V_{out}(\omega) = 0\]

Note: The ignored quantities need not be small.
Colpitts Oscillator: Small Signal Model

\[
\begin{bmatrix}
  j\omega L + \frac{1}{j\omega C_1C_2} + R - \frac{g_m}{\omega^2 C_1C_2}
\end{bmatrix} = 0
\]

This implies:

\[
j\omega L + \frac{1}{j\omega C_1C_2} + R = \frac{g_m}{\omega^2 C_1C_2}
\]

and:

\[
R = \frac{g_m}{\omega^2 C_1C_2} = \frac{L}{C_1C_2}
\]

The above implies that the FET gain must balance the dissipation due to the resistor \( R \).

Electrical Oscillators: Another Viewpoint

Consider the following LCR circuit:

Doing KCL at node (1) gives:

\[
\begin{bmatrix}
  j\omega L + \frac{1}{j\omega C} -\frac{G}{j\omega C} + R - \frac{L}{C}
\end{bmatrix} v_{out}(\omega) = 0
\]

This implies:

\[
j\omega L + \frac{1}{j\omega C} = 0
\]

and:

\[
R = \frac{L}{C}
\]

The above implies that the gain must balance the dissipation due to the resistor \( R \).
Consider the following cross-connected differential pair:

Suppose we find the differential resistance looking into the terminals A and B ..........

We have:
\[ v_{o2} - v_{o1} = v_f \]
\[ v_{gs1} - v_{gs2} = v_f = v_{id} \]

Therefore:
\[ i_{d1} = g_m \frac{v_f}{2} \]
\[ i_{d2} = -g_m \frac{v_f}{2} \]

And KCL gives at (1) and (2):
\[ i_{d1} + i_t + \frac{v_{o1}}{R} = 0 \]
\[ i_{d2} - i_t + \frac{v_{o2}}{R} = 0 \]

Subtracting the above two gives:
\[ \frac{v_f}{i_t} = \frac{2R}{1 - g_m R} = \left( 2R \parallel \frac{2}{g_m} \right) = -\frac{2}{g_m} \]

Forget the output conductance of the FETs for now
A Differential Pair Negative Resistance Element

KCL gives:

\[
g_m v_{gs1} + g_d (v_{o1} - v_s) + i_t = -\frac{v_{o1}}{R}
\]

\[
g_m v_{gs2} + g_d (v_{o2} - v_s) - i_t = -\frac{v_{o2}}{R}
\]

Subtracting the two gives:

\[
g_m v_t - g_d v_t + 2i_t = \frac{v_t}{R}
\]

\[
g_m v_t + g_d v_t + 2i_t = \frac{v_t}{R}
\]

\[
\Rightarrow i_t = \frac{2R}{1 - (g_m - g_d)R} = \left(2R \parallel \frac{2}{g_m - g_d}\right) = \left(2R \parallel \frac{2}{g_m}\right)
\]

A Differential Pair Negative Resistance Element

Equivalent small signal model

\[
\frac{v_t}{i_t} = \frac{2R}{1 - g_m R} = \left(2R \parallel \frac{2}{g_m}\right) \approx \frac{2}{g_m}
\]

Resistance = \frac{2}{g_m}
A Differential Pair Negative Resistance Element

Consider the following cross-connected differential pair:

\[
\frac{v_t}{i_t} = \left(2R || 2r_o \parallel \frac{2}{g_m}\right) \approx \frac{2}{g_m}
\]

Now with FET output conductance included.

A Differential Pair Oscillator

Parasitic
A Differential Pair Oscillator

Consider the following cross-connected differential pair:

\[
\begin{align*}
2L & \quad 2L \\
2R & \quad 2L
\end{align*}
\]

Parasitic

\[
2g_m \quad \frac{2g_m}{g_m} \quad \frac{L}{C} \quad \frac{L}{C}
\]

\[g_m r_o \gg 1\]

\[
\left[j\omega L + \frac{1}{j\omega C} \left(\frac{g_m R}{2} - \frac{L}{C}\right)\right] v_{out}(\omega) = 0
\]

\[j\omega L + \frac{1}{j\omega C} = 0\]

\[\Rightarrow \omega = \frac{1}{\sqrt{LC}}\]

A Higher Gain Differential Pair Oscillator

\[
\begin{align*}
2g_m & \quad \frac{2g_m}{g_m} \\
g_{mp} & \quad \frac{g_{mp}}{g_{mp}}
\end{align*}
\]

\[
2g_{mn} \quad \frac{2g_{mn}}{g_{mn}} \quad \frac{L}{C} \quad \frac{L}{C}
\]

\[
j\omega L + \frac{1}{j\omega C} = 0\]

\[\Rightarrow \omega = \frac{1}{\sqrt{LC}}\]

\[R = \frac{g_{mn} + g_{mp} L}{2C}\]
Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs)

### ADC

<table>
<thead>
<tr>
<th>Analog input</th>
<th>Digital Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>$N$-bits</td>
</tr>
<tr>
<td>$V_{MIN} &lt; V_{IN} &lt; V_{MAX}$</td>
<td></td>
</tr>
</tbody>
</table>

**Resolution:**

$$\frac{V_{MAX} - V_{MIN}}{2^N - 1}$$

**Dynamic Range:**

$$20\log_{10}\left(\frac{V_{MAX}}{V_{MIN}}\right)$$

### DAC

<table>
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<tbody>
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<td>$N$-bits</td>
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</table>

Analog-to-Digital Converters (ADCs)

$$V_{IN}(t)$$

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<tbody>
<tr>
<td></td>
<td>$N$-bits</td>
</tr>
</tbody>
</table>

**Logical 0 ↔ $V_{LOW}$**

**Logical 1 ↔ $V_{HIGH}$**

Most significant bit (MSB)

Least significant bit (LSB)

Analog value, corresponding to a digital value, is:

$$V_{MIN} + \frac{(V_{MAX} - V_{MIN})}{(2^N - 1)} [2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots + 2^2B_2 + 2^1B_1 + B_0]$$
Sample and Hold in Analog-to-Digital Converters (ADCs)

Sample the input waveform periodically and hold the sampled value in place till the next sampling event.

Anti-Aliasing Filter in Analog-to-Digital Converters (ADCs)

Noise outside the signal band gets “aliased” into the signal band upon sampling.

Anti-aliasing filter

Frequency ($\omega$)
Sample and Hold in Analog-to-Digital Converters (ADCs)

1) Input impedance not large enough
2) Output could have an offset
3) Capacitor can take a long time to charge/discharge

A Better Sample and Hold Circuit

\[ V_I = A_1 (V_S - V_{IN}) \]

Large input impedance
Output offset problem solved

Suppose when the CLK is HIGH the current through the FET is (assuming linear region):

\[ I_D = k_n \left( V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS} \approx k_n (V_{CLK} - V_{TN}) V_I - \frac{V_I}{R_n} \]

Then:

\[ C \frac{d(0 - V_S)}{dt} = I_D = \frac{V_I}{R_n} = \frac{A_1 (V_S - V_{IN})}{R_n} \]

\[ \Rightarrow \frac{dV_S}{dt} + \frac{A_1}{R_n C} V_S = \frac{A_1}{R_n} V_{IN} \]

\[ \Rightarrow V_S(t) = V_S(0) e^{-\frac{A_1}{R_n C} t} + V_{IN} \left( 1 - e^{-\frac{A_1}{R_n C} t} \right) \]

\( V_S \) is pulled to 0 V and \( V_I \) is pulled to \(-0 \) V within a very short time after CLK goes HIGH
3-bit Flash ADC

Voltage resolution:
\[ \Delta V = \frac{V_{\text{MAX}} - V_{\text{MIN}}}{2^N - 1} \]

Pros:
- Very high speed architecture

Cons:
- Component intensive (requires \(2^N-1\) comparators)

Voltage comparators are essentially diff amps that have very low voltage offset errors; the input voltage offset error needs to be much less than the resolution of the ADC.

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs)

Internal register keeps updating the stored digital value, compares the resulting analog value obtained from this digital value to the input analog value, until the stored value matches the input value. And then the stored value is placed in the output register.
Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs)

Consider a 4-bit SAR-ADC with a 0-3 V input range

0000 => 0 Volts            1111 => 3 Volts

Resolution = 0.2 Volt

Suppose the input is 1.70 Volts

Start

SAR = 1000 → DAC = 1.60 V → Error = +1 → Stored value is smaller
SAR = 1111 → DAC = 3.00 V → Error = -1 → Stored value is larger
SAR = 1100 → DAC = 2.40 V → Error = +1 → Stored value is larger
SAR = 1010 → DAC = 2.00 V → Error = +1 → Stored value is larger
SAR = 1001 → DAC = 1.80 V → Error = +1 → Stored value is larger

Produce output

Pros: Scalable to high resolutions  Cons: Slower than flash

Pipelined Analog-to-Digital Converters (ADCs)

Main Idea: Use features of the flash architecture but scale to higher resolutions

Example: Build a 6-bit pipelined ADC from two 3-bit Flash ADCs
Pipelined Analog-to-Digital Converters (ADCs)

Can easily generalize:

\[ V(t) \]

Pros:
- Scalable to high resolutions
- Fast

Cons:
- Large power dissipation

Analog-to-Digital Converters (ADCs): State of the Art
R/2R Ladder Digital-to-Analog Converters (DACs)

\[ V_C = V_{HIGH} \left( \frac{B_{N-1}}{2} + \frac{B_{N-2}}{4} + \frac{B_{N-3}}{8} + \ldots + \frac{B_2}{2^{N-2}} + \frac{B_1}{2^{N-1}} + \frac{B_0}{2^N} \right) \]

If:

\[ A = \left( V_{MAX} - V_{MIN} \right) \frac{2^N}{V_{HIGH}} \]

Then the output will be the desired analog output:

\[ V_{OUT} = V_{MIN} + \left( V_{MAX} - V_{MIN} \right) \left[ \frac{2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots + 2^2B_2 + 2^1B_1 + B_0}{2^N - 1} \right] \]

Thermometer Code Digital-to-Analog Converters (DACs)

\[ V_C = IR(D_{2^{N-1}} + D_{2^{N-2}} + \ldots + D_1 + D_0) \]

\[ V_C = IR\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots + 2^2B_2 + 2^1B_1 + B_0\right] \]

\[ V_{OUT} = V_{MIN} + \left( V_{MAX} - V_{MIN} \right) \left[ \frac{2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots + 2^2B_2 + 2^1B_1 + B_0}{2^N - 1} \right] \]
Switching Mixers: Why?

- Silicon development is driven by digital
- With better digital comes smaller faster devices
- These trends are bad for many analog designs
  - Lower headroom, worse channel length modulation, velocity saturation, etc
- What does get better are switches!
Switching Mixer: Basics

Say the switch opens and closes with LO

We know that when the switch is open:

\[ I_{RF} = 0 \]

When the switch is closed:

\[ I_{RF} = \frac{V_{RF}}{R_S + R_L} \]

We can therefore write the overall current as:

\[ I_{RF} = \frac{V_{RF}}{R_S + R_L} \times LO \]

Where LO is a square wave with amplitude 1 and frequency \( f_{LO} \).
Switching Mixer: Basics Cont.

Writing the overall current as:

\[ I_{RF} = \frac{V_{RF}}{R_s + R_L} \times LO \]

Doing a Fourier series expansion on LO gives us:

\[ LO(t) = \frac{1}{2} + \frac{2}{\pi} \left[ \sin(\omega_{LO}t) + \frac{\sin(3\omega_{LO}t)}{3} + \frac{\sin(5\omega_{LO}t)}{5} + \ldots \right] \]

If we take:

\[ V_{RF} = A \cos(\omega_{RF}t) \]

Then we can see that the overall current is:

\[ I_{RF}(t) = \frac{A \cos(\omega_{RF}t)}{2(R_s + R_L)} + \frac{2A}{\pi(R_s + R_L)} \left[ \cos(\omega_{RF}t) \sin(\omega_{LO}t) + \frac{\cos(\omega_{RF}t) \sin(3\omega_{LO}t)}{3} + \frac{\cos(\omega_{RF}t) \sin(5\omega_{LO}t)}{5} + \ldots \right] \]
Switching Mixer: Basics Cont.

We have just seen that the current through the switch is:

\[ I_{RF}(t) = \frac{A \cos(\omega_{RF}t)}{2(R_S+R_L)} + \frac{2A}{\pi(R_S+R_L)} \left[ \cos(\omega_{RF}t) \sin(\omega_{LO}t) + \frac{\cos(\omega_{RF}t) \sin(3\omega_{LO}t)}{3} + \frac{\cos(\omega_{RF}t) \sin(5\omega_{LO}t)}{5} + ... \right] \]

If we were to look at the voltage across \( R_L \) we would see our multiplied tones and many harmonics!

Due to this we typically apply filtering to the the voltage across \( R_L \) as follows:

![Circuit Diagram]

Cbb forms a short for any high frequencies so only low frequency voltages appear across \( R_L \).
Switching Mixer: Issues

In addition to doing down and up conversion around the fundamental tone we also get conversion near our harmonics.

The down conversion of harmonics can be very detrimental to mixer performance. Harmonic Down conversion can be thought of as aliasing and causes more noise to be down converted.

Harmonics can be rejected if we switch to a multiphase topology.

For those interested in multiphase mixers more information can be found in the paper:

"Implications of Passive Mixer Transparency for Impedance Matching and Noise Figure in Passive Mixer-First Receivers,"

On Professor Molnar’s Website

Image from: C. Andrews and A. C. Molnar,