The Need for Multistage Amplifiers

Most modern amplifiers have multiple stages. Some reasons are:

1) Increase the amplifier gain (voltage gain or current gain or transimpedance gain or transconductance gain)
2) Transform the input resistance to match the source
3) Transform the output resistance to match the load
4) Allow large voltage swings at the output
5) Meet other specs (on frequency performance, noise, stability, etc)
A Cascade of Two CS Stages for a Voltage Amplifier

\[ V_{DD} \]

\[ r_{oc1} \]

\[ I_{BIAS1} \]

\[ I_{D1} \]

\[ M1 \]

\[ V_{BIAS} + V_s \]

\[ R_s \]

\[ + \]

\[ V_{OUT} + v_{out} \]

\[ - \]

\[ R_L \]

\[ V_{DD} \]

\[ r_{oc2} \]

\[ I_{BIAS2} \]

\[ I_{D2} \]

\[ M2 \]

\[ + \]

\[ - \]

A Cascade of Two CS Stages for a Voltage Amplifier

\[ V_{DD} \]

\[ r_{oc1} \]

\[ I_{BIAS1} \]

\[ I_{D1} \]

\[ M1 \]

\[ v_{in1} + R_{in1} \]

\[ A_v v_{in1} \]

\[ + \]

\[ - \]

\[ R_{out1} \]

\[ v_{out} \]

\[ 1 \]

\[ 2 \]

\[ V_{DD} \]

\[ r_{oc2} \]

\[ I_{BIAS2} \]

\[ I_{D2} \]

\[ M2 \]

\[ v_{in2} + R_{in2} \]

\[ A_v v_{in2} \]

\[ + \]

\[ - \]

\[ R_{out2} \]

\[ v_{out} \]
A Cascade of Two CS Stages: Finding Input Resistances (Work Your Way Backwards)

1) First find $R_{in2}$ (input resistance of the last stage):
   Make sure $R_L$ is in place!!
   \[ R_{in2} = \infty \]

2) Then find $R_{in1}$ (input resistance of the second last stage):
   Make sure $R_{in2}$ is in place!!
   \[ R_{in1} = \infty \]

A Cascade of Two CS Stages: Finding Output Resistances (Work Your Way Forwards)

1) First find $R_{out1}$ (output resistance of the first stage):
   Make sure $R_S$ is in place!!
   \[ R_{out1} = (r_{o1} \parallel r_{oc1}) \]

2) Then find $R_{out2}$ (output resistance of the second stage):
   Make sure $R_{out1}$ is in place!!
   \[ R_{out2} = (r_{o2} \parallel r_{oc2}) \]
A Cascade of Two CS Stages: Finding Voltage Gains

1) Open circuit voltage gains of CS stages do not depend on how the stages are connected (i.e. on source or load resistances)

Stage 1 Parameters:

\[ R_{i1} = \infty \]
\[ R_{o1} = (r_{o1} \parallel r_{oc1}) \]
\[ A_{v1} = -g_{m1}(r_{o1} \parallel r_{oc1}) \]

Stage 2 Parameters:

\[ R_{i2} = \infty \]
\[ R_{o2} = (r_{o2} \parallel r_{oc2}) \]
\[ A_{v2} = -g_{m2}(r_{o2} \parallel r_{oc2}) \]

A Cascade of Two Amplifiers

Open circuit voltage gain:

\[ v_{out} = A_{v2}v_{in2} = A_{v2}A_{v1}v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \]
\[ = A_{v2}A_{v1}v_{in} \frac{R_{in2}}{R_{out1} + R_{in2}} \]
\[ \Rightarrow A_{v} = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} \]

Inter-stage voltage divider
A Cascade of Two Amplifiers

The two stages can be combined into an equivalent single stage model:

Open circuit voltage gain:
\[ A_v = \frac{v_{out}}{v_{in}} = \frac{A_1 A_2 R_{in2}}{R_{out1} + R_{in2}} \]

Inter-stage voltage divider

A Cascade of Two Amplifiers with a Source Resistor

Voltage gain:
\[ v_{out} = A_2 v_{in2} \frac{R_L}{R_{out2} + R_L} = A_2 A_1 v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

\[ = A_2 A_1 v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

For the CS FET stages:
\[ R_{in1} = R_{in2} = \infty \]

Input voltage divider
Inter-stage voltage divider
Output voltage divider
A Cascade of Two Amplifiers with a Source Resistor

\[ v_{out} = A_v v_{in} + \frac{R_L}{R_{out2} + R_L} \]

One can also use the equivalent single stage mode to find the voltage gain:

\[ v_{out} = A_v v_{in} \]

It is easier to use the single-stage model

Input voltage divider

Output voltage divider

The final expression is the same as the one on the previous slide

A Cascade of Two CS Stages for a Voltage Amplifier

Putting it all together:

Input resistance:
\[ R_{in} = \infty \]

Output resistance:
\[ R_{out} = r_{o2} \parallel r_{oc2} \]

Open circuit voltage gain:
\[ A_v = \frac{v_{out}}{v_{in}} = A_1 A_2 \frac{R_{in2}}{R_{out1} + R_{in2}} \]

Not really a good voltage amplifier – output resistance is too large – but a decent transconductance amplifier
A Cascade of Three FET Stages: 2 CS and 1 CD

Input resistance:
\[ R_{in} = \infty \]

Output resistance:
\[ \frac{1}{R_{out}} \approx \frac{1}{r_{oc3} + (g_{m3} + g_{mb3})} \approx (g_{m3} + g_{mb3}) \]

Open circuit voltage gain:
\[ A_v = A_v1A_v2A_v3 \approx (-g_{m1}(r_{o1} \parallel r_{oc1}))(-g_{m2}(r_{o2} \parallel r_{oc2}))[-1] \]

Why?

Now it is a better voltage amplifier!

A Cascade of Three FET Stages: DC Biasing

In the above scheme, the DC bias of one stage affects the DC bias of another stage.

Need to ensure appropriate DC bias of every stage such that:

i) The FETs are operating in saturation

ii) The desired voltage swing does not cause problems (e.g. cause some FET to go out of saturation)
A Cascade of Three FET Stages: Current Source Biasing

The sizes (W/L ratios) of M4, M5, and M6 can be adjusted to get the desired bias currents for the three amplifier stages.

A Cascade of CS and CG: A Capacitively-Coupled Cascode

The FET cascode has a large input resistance, a very large output resistance, and a large gain.

But it is much better than a CS-CS cascade in terms of the frequency performance, as we will see later in the course.

The above topology can be simplified…….
A Cascade of CS and CG: A Direct-Coupled Cascode

One current source can bias both the stages in a direct-coupling topology....!

This is the preferred way for on-chip designs

A Cascade of CS and CG: The Cascode

A different way to draw the same circuit
The FET Cascode: Input and Output Resistances of Each Stage

Input resistances:
\[ R_{in2} \approx \frac{1}{g_{m2} + g_{mb2}} (1 + \frac{r_{oc}}{r_{o2}}) \]
\[ R_{in1} = \infty \]

\[ \Rightarrow R_{in} = R_{in1} = \infty \]

Output resistances:
\[ R_{out1} = r_{o1} \]
\[ R_{out2} = r_{oc} || \left[ r_{o2} + R_{out1} + r_{o2} (g_{m2} + g_{mb2}) R_{out1} \right] \approx r_{oc} || \left[ (g_{m2} + g_{mb2}) r_{o1} r_{o2} \right] \]
\[ \Rightarrow R_{out} = R_{out2} \approx r_{oc} || \left[ (g_{m2} + g_{mb2}) r_{o1} r_{o2} \right] \]

The FET Cascode: Voltage Gains of Each Stage

Voltage Gains:
\[ A_{v1} = -g_{m1} r_{o1} \]
\[ A_{v2} = \left( g_{m2} + g_{mb2} + \frac{1}{r_{o2}} \right) \left( r_{o2} || r_{oc} \right) \]
\[ \Rightarrow A_{v} = \frac{V_{out}}{V_{in}} = A_{v2} A_{v1} = \frac{R_{in2}}{R_{out1} + R_{in2}} = \left( -g_{m1} r_{o1} \right) \left[ (g_{m2} + g_{mb2}) r_{o2} + 1 \right] \frac{r_{oc}}{r_{o2} + r_{oc} \left[ (g_{m2} + g_{mb2}) r_{o1} r_{o2} \right]} + 1 \]

If \( r_{oc} \gg r_{o2}, r_{o1} \):
\[ A_{v} = \left[ -g_{m1} r_{o1} \right] \left[ (g_{m2} + g_{mb2}) r_{o2} + 1 \right] = \left[ -g_{m1} r_{o1} \right] \left[ (g_{m2} + g_{mb2}) r_{o2} \right] \]
\[ \Rightarrow \text{Very large} \]
**The FET Cascode: Voltage Gains of Each Stage**

Voltage Gains:

- \( A_{v1} = -g_m r_{o1} \)
- \( A_{v2} = (g_m + g_{mb2})(r_{o2} || r_{oc}) \)

\[
A_v = \frac{v_{out}}{v_{in}} = A_{v2} A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} \approx \left( -g_m r_{o1} \right) \left( g_m + g_{mb2} \right) \frac{r_{o2} r_{oc}}{r_{o2} + r_{oc}} \left( g_m + g_{mb2} \right) \frac{r_{o1} r_{oc}}{r_{o2} + r_{oc}}
\]

If \( r_{oc} \approx r_{o2}, r_{o1} \):

\[
A_v \approx \left( -g_m r_{o1} \right) \left( g_m + g_{mb2} \right) \frac{r_{o2} r_{oc}}{r_{o2} + r_{oc}} \left( g_m + g_{mb2} \right) \frac{r_{o1} r_{oc}}{r_{o2} + r_{oc}}
\]

\( A_v \approx -g_m r_{oc} \)  

Can still be large

---

**The FET Cascode: Transconductance Gain**

Transconductance Gain (with output shorted):

\[
G_m = \frac{i_{out}}{v_{in}} = \frac{A_v}{R_{out}} \approx -g_{m1}
\]
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = I_{BIAS} \]

Problem: To be accurate with voltage biasing, one needs to know the characteristics (i.e. \( k_n \), \( k_p \), etc) of the FETs accurately, and this information is usually not available to the circuit designer.

Solution: Use circuit biasing schemes that are not too sensitive to the circuit designer's detailed knowledge of the FETs!
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = -I_{D3} = \ldots = -I_{D4} = I_{BIAS} \]

Need to realize this voltage source

\[ V_{BIAS2} \]

\[ V_{BIAS1} + V_{in} \]

M4 and M3 are matched

Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = -I_{D3} = \ldots = -I_{D4} = I_{BIAS} \]

Need to realize this voltage source

\[ V_{BIAS2} \]

\[ V_{BIAS1} + V_{in} \]

M4 and M3 are matched
Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = -I_{D3} = \ldots \]
\[ = -I_{D4} = I_{D5} = \ldots \]
\[ = I_{BIAS} \]

What if we have only a single stable current source available on the chip..?
Biasing the FET Cascode Amplifier

Current mirror

M4 and M3 are matched

M5 and M2 are matched

FET voltage source

PFET current source (does not have large enough $r_{oc}$)

Improved FET Cascode Amplifier

Current mirror

M4 and M3 are matched

M5 and M2 are matched

FET voltage source

Cascode PFET current source

M9 and M8 are matched

M4 and M3 are matched

M5 and M2 are matched

Cascode PFET current source