Lecture 15

Multistage FET Amplifiers

In this lecture you will learn:

• Multistage FET Amplifiers
• The Cascade Design
• The Cascode Design
• DC Biasing FET Amplifiers

The Need for Multistage Amplifiers

Most modern amplifiers have multiple stages. Some reasons are:

1) Increase the amplifier gain (voltage gain or current gain or transimpedance gain or transconductance gain)

2) Transform the input resistance to match the source

3) Transform the output resistance to match the load

4) Allow large voltage swing at the output
A Cascade of Two CS Stages for a Voltage Amplifier

\[ V_{ID1} \]
\[ V_{ID2} \]
\[ V_{DD} \]
\[ I_{BIAS1} \]
\[ I_{BIAS2} \]
\[ V_{BIAS} + V_s \]
\[ R_s \]
\[ R_{L} \]
\[ M1 \]
\[ M2 \]

\[ v_{in1} \]
\[ R_{in1} \]
\[ R_{out1} \]
\[ A_1 v_{in1} \]

\[ v_{in2} \]
\[ R_{in2} \]
\[ R_{out2} \]
\[ A_2 v_{in2} \]

\[ v_{out} \]
A Cascade of Two CS Stages: Finding Input Resistances (Work Your Way Backwards)

1) First find $R_{in2}$ (input resistance of the last stage):
   - Make sure $R_L$ is in place!!
   - $R_{in2} = \infty$

2) Then find $R_{in1}$ (input resistance of the second last stage):
   - Make sure $R_{in2}$ is in place!!
   - $R_{in1} = \infty$

A Cascade of Two CS Stages: Finding Output Resistances (Work Your Way Forward)

1) First find $R_{out1}$ (output resistance of the first stage):
   - Make sure $R_S$ is in place!!
   - $R_{out1} = (r_{o1} \parallel r_{oc1})$

2) Then find $R_{out2}$ (output resistance of the second stage):
   - Make sure $R_{out1}$ is in place!!
   - $R_{out2} = (r_{o2} \parallel r_{oc2})$
A Cascade of Two CS Stages: Finding Voltage Gains

1) Open circuit voltage gains of CS stages do not depend on how the stages are connected (i.e. on source or load resistances)

Stage 1 Parameters:
\[ R_{in1} = \infty \]
\[ R_{out1} = (r_{o1} \| r_{oc1}) \]
\[ A_{v1} = -g_{m1}(r_{o1} \| r_{oc1}) \]

Stage 2 Parameters:
\[ R_{in2} = \infty \]
\[ R_{out2} = (r_{o2} \| r_{oc2}) \]
\[ A_{v2} = -g_{m2}(r_{o2} \| r_{oc2}) \]

A Cascade of Two Amplifiers

Open circuit voltage gain:
\[ v_{out} = A_{v2}v_{in2} = A_{v2}A_{v1}v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \]
\[ = A_{v2}A_{v1}v_{in} \frac{R_{in2}}{R_{out1} + R_{in2}} \]
\[ \Rightarrow A_{v} = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} \]

Inter-stage voltage divider
A Cascade of Two Amplifiers

The two stages can be combined into an equivalent single stage model:

Open circuit voltage gain:

\[ A_v = \frac{v_{out}}{v_{in}} = A_{221} A_{112} \frac{R_{in2}}{R_{out1} + R_{in2}} \]

Inter-stage voltage divider

A Cascade of Two Amplifiers with a Source Resistor

Voltage gain:

\[ v_{out} = A_{221} v_{in2} \frac{R_L}{R_{out2} + R_L} = A_{221} A_{112} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

\[ = A_{221} A_{112} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_{in2}}{R_{out2} + R_L} \]

\[ = A_{221} A_{112} v_{s} \frac{R_{in1}}{R_s + R_{in1}} \frac{R_{in2}}{R_{out2} + R_L} \]

\[ \Rightarrow \frac{v_{out}}{v_s} = A_{221} A_{112} \frac{R_{in1}}{R_s + R_{in1}} \frac{R_{in2}}{R_{out2} + R_L} \]

Input voltage divider  Inter-stage voltage divider  Output voltage divider

For the CS FET stages:

\[ R_{in1} = R_{in2} = \infty \]
A Cascade of Two Amplifiers with a Source Resistor

One can also use the equivalent single stage mode to find the voltage gain:

\[ v_{\text{out}} = A_v v_{\text{in}} \frac{R_L}{R_{\text{out2}} + R_L} \]

\[ = A_v v_s \frac{R_{\text{in1}}}{R_s + R_{\text{in1}} R_{\text{out2}} + R_L} \]

\[ \Rightarrow v_{\text{out}} \frac{v_s}{v_s} = A_v \frac{R_{\text{in1}}}{R_s + R_{\text{in1}} R_{\text{out2}} + R_L} \]

It is easier to use the single-stage model

The final expression is the same as the one on the previous slide

Input voltage divider

Output voltage divider

A Cascade of Two CS Stages for a Voltage Amplifier

Putting it all together:

Input resistance:

\[ R_{\text{in}} = \infty \]

Output resistance:

\[ R_{\text{out}} = r_{o2} || r_{oc2} \]

Open circuit voltage gain:

\[ \frac{v_{\text{out}}}{v_{\text{in}}} = A_v = A_1 A_2 \frac{R_{\text{in2}}}{R_{\text{out1}} + R_{\text{in2}}} \]

\[ = \left[ -g_m(r_1 || r_{oc1}) \right] \left[ -g_m(r_2 || r_{oc2}) \right] \]

Not really a good voltage amplifier – output resistance is too large – but a decent transconductance amplifier
A Cascade of Three FET Stages: 2 CS and 1 CD

Input resistance:
\[ R_{\text{in}} = \infty \]

Output resistance:
\[ \frac{1}{R_{\text{out}}} \approx \frac{1}{r_{oc3} \left( g_{m3} + g_{mb3} \right)} \approx \left( g_{m3} + g_{mb3} \right) \]

Open circuit voltage gain:
\[ A_v = A_{v1} A_{v2} A_{v3} \]
\[ = \left[ -g_{m1}(r_{oc1}) \right] \left[ -g_{m2}(r_{oc2}) \right] \approx -1 \]

Now it is a better voltage amplifier!

A Cascade of Three FET Stages: DC Biasing

In the above scheme, the DC bias of one stage affects the DC bias of another stage.

Need to ensure appropriate DC bias of every stage such that:

i) The FETs are operating in saturation
ii) The desired voltage swing does not cause problems (e.g. cause some FET to go out of saturation)
### A Cascade of Three FET Stages: Current Source Biasing

The sizes (W/L ratios) of M4, M5, and M6 can be adjusted to get the desired bias currents for the three amplifier stages.

### A Cascade of CS and CG: A Capacitively-Coupled Cascode

The FET cascode has a large input resistance, a very large output resistance, and a large gain.

But it is much better than a CS-CS cascade in terms of the frequency performance, as we will see later in the course.

The above topology can be simplified........
A Cascade of CS and CG: A Direct-Coupled Cascode

One current source can bias both the stages in a direct-coupling topology....

This is the preferred way for on-chip designs.

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A Cascade of CS and CG: The Cascode

A different way to draw the same circuit.
The FET Cascode: Input and Output Resistances of Each Stage

Input resistances:

\[ R_{\text{in2}} \approx \frac{1}{g_{m2} + g_{mb2}} \left( 1 + \frac{r_{oc}}{r_{o2}} \right) \]

Assuming \( R_c = \infty \)

\[ R_{\text{in1}} = \infty \]

\[ \Rightarrow R_{\text{in}} = R_{\text{in1}} = \infty \]

Output resistances:

\[ R_{\text{out1}} = r_{o1} \]

\[ R_{\text{out2}} = r_{oc} \parallel \left[ r_{o2} + r_{out1} \parallel r_{o2} \left( g_{m2} + g_{mb2} \right) R_{\text{out1}} \right] \approx r_{oc} \parallel [(g_{m2} + g_{mb2})r_{o1}r_{o2}] \]

\[ \Rightarrow R_{\text{out}} = R_{\text{out2}} = r_{oc} \parallel [(g_{m2} + g_{mb2})r_{o1}r_{o2}] \]

The FET Cascode: Voltage Gains of Each Stage

Voltage Gains:

\[ A_{V1} = -g_{m1}r_{o1} \]

\[ A_{V2} = \left( g_{m2} + g_{mb2} + \frac{1}{r_{o2}} \right) \left( r_{o2} \parallel r_{oc} \right) \approx \left( g_{m2} + g_{mb2} \right) \left( r_{o2} \parallel r_{oc} \right) \]

\[ \Rightarrow A_v = \frac{v_{\text{out}}}{v_{\text{in}}} = A_{V2}A_{V1} \frac{R_{\text{in2}}}{R_{\text{out1}} + R_{\text{in2}}} = (-g_{m1}r_{o1}) \left( g_{m2} + g_{mb2} \right) \left( r_{o2} \parallel r_{oc} \right) \frac{r_{o2}r_{oc}}{r_{o2} + r_{oc}} \frac{1}{(g_{m2} + g_{mb2})r_{o1}r_{o2} + r_{oc}} \]

If \( r_{oc} \gg r_{o2}, r_{o1} \):

\[ \Rightarrow A_v = [-g_{m1}r_{o1}] [(g_{m2} + g_{mb2})r_{o2}] \rightarrow \text{Very large} \]
### The FET Cascode: Voltage Gains of Each Stage

**Voltage Gains:**

\[ A_{V1} = -g_{m1}r_{o1} \quad A_{V2} = (g_{m2} + g_{mb2})(r_{o2} || r_{oc}) \]

\[ A_V = \frac{v_{out}}{v_{in}} = \frac{A_{V2}A_{V1}}{R_{out2} + R_{in2}} \approx -\frac{g_{m1}r_{o1}r_{o2}r_{oc}}{(g_{m2} + g_{mb2})r_{o2} + r_{oc}} \]

If \( r_{oc} \approx r_{o2}, r_{o1} \):

\[ A_V \approx \frac{r_{o2}r_{oc}}{r_{o2} + r_{oc}} \frac{1}{(g_{m2} + g_{mb2})r_{o1}r_{o2} + r_{oc}} \]

\[ A_V = -g_{m1}r_{oc} \quad \text{Can still be large} \]

### The FET Cascode: Transconductance Gain

**Transconductance Gain (with output shorted):**

\[ G_m = \frac{i_{out}}{v_{in}} = \frac{A_v}{R_{out}} \approx -g_{m1} \]
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = I_{BIAS} \]

Need to realize this voltage source

\[ V_{BIAS1} + v_{in} \]

M1

M2

\[ I_{D2} \]

\[ V_{OUT} + v_{out} \]

Need to realize this current source

\[ I_{BIAS} \]

M3

Use a PFET to implement the current source

\[ V_{BIAS3} \]

\[ I_{D3} \]

Problem: To be accurate with voltage biasing, one needs to know the characteristics (i.e. \( k_n \), \( k_p \), etc) of the FETs accurately, and this information is usually not available to the circuit designer.

Solution: Use circuit biasing schemes that are not too sensitive to the circuit designer's detailed knowledge of the FETs!
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = -I_{D3} = ... = -I_{D4} = I_{BIAS} \]

Need to realize this voltage source

\[ V_{BIAS1} + V_{IN} \]

M4 and M3 are matched

Current mirror

M4 and M3 are matched

M4 and M3 are matched
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = -I_{D3} = \ldots = -I_{D4} = I_{D5} = \ldots = I_{BIAV} \]

What if we have only a single stable current source available on the chip..?

Biasing the FET Cascode Amplifier

Resistance looking into a voltage source must be small.
Biasing the FET Cascode Amplifier

**Current mirror**
- M4 and M3 are matched
- M5 and M2 are matched
- M4 and M3 are matched
- M5 and M2 are matched

**PFET current source**
- (does not have large enough $r_{oc}$)

**FET voltage source**
- M9 and M8 are matched
- M4 and M3 are matched

Improved FET Cascode Amplifier

**Current mirror**
- M4 and M3 are matched
- M5 and M2 are matched

**Cascode PFET current source**
- M9 and M8 are matched
- M4 and M3 are matched
- M5 and M2 are matched