

## Lecture 15

### Multistage FET Amplifiers

---

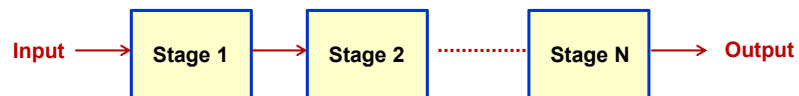
In this lecture you will learn:

- Multistage FET Amplifiers
- The Cascade Design
- The Cascode Design
- DC Biasing FET Amplifiers

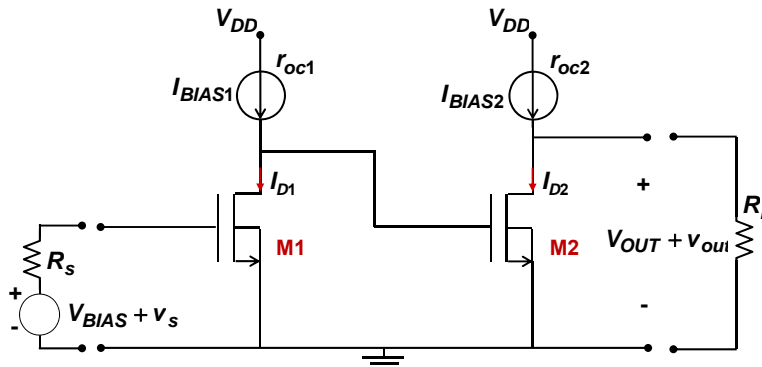
### The Need for Multistage Amplifiers

Most modern amplifiers have multiple stages. Some reasons are:

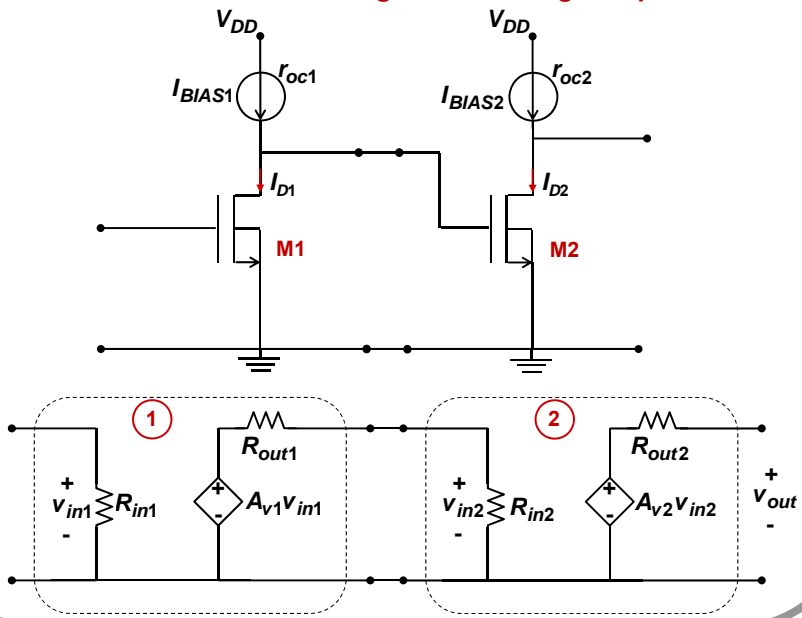
- 1) Increase the amplifier gain (voltage gain or current gain or transimpedance gain or transconductance gain)
- 2) Transform the input resistance to match the source
- 3) Transform the output resistance to match the load
- 4) Allow large voltage swings at the output
- 5) Meet other specs (on frequency performance, noise, stability, etc)



### A Cascade of Two CS Stages for a Voltage Amplifier

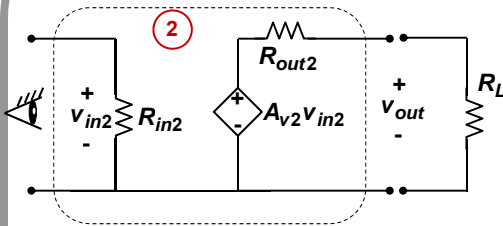


### A Cascade of Two CS Stages for a Voltage Amplifier



### A Cascade of Two CS Stages: Finding Input Resistances (Work Your Way Backwards)

1)



1) First find  $R_{in2}$  (input resistance of the last stage):

Make sure  $R_L$  is in place!!

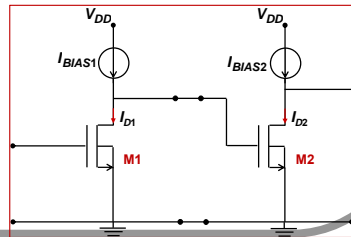
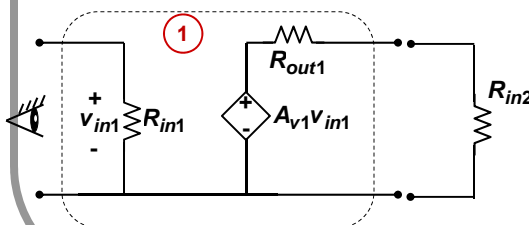
$$R_{in2} = \infty$$

2) Then find  $R_{in1}$  (input resistance of the second last stage):

Make sure  $R_{in2}$  is in place!!

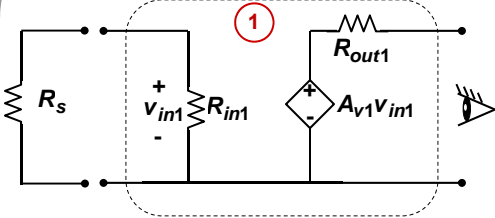
$$R_{in1} = \infty$$

2)



### A Cascade of Two CS Stages: Finding Output Resistances (Work Your Way Forwards)

1)



1) First find  $R_{out1}$  (output resistance of the first stage):

Make sure  $R_s$  is in place!!

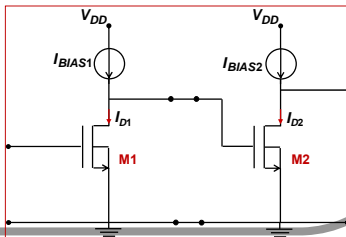
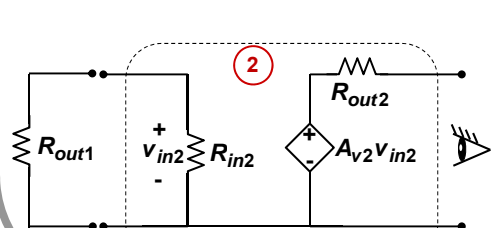
$$R_{out1} = (r_{o1} \parallel r_{oc1})$$

2) Then find  $R_{out2}$  (output resistance of the second stage):

Make sure  $R_{out1}$  is in place!!

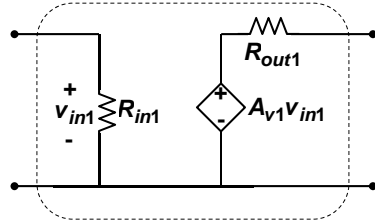
$$R_{out2} = (r_{o2} \parallel r_{oc2})$$

2)



## A Cascade of Two CS Stages: Finding Voltage Gains

1)

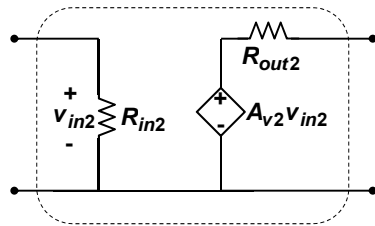


Open circuit voltage gains of CS stages do not depend on how the stages are connected (i.e. on source or load resistances)

Stage 1 Parameters:

$$\begin{aligned} R_{in1} &= \infty \\ R_{out1} &= (r_{o1} \parallel r_{oc1}) \\ A_{v1} &= -g_{m1}(r_{o1} \parallel r_{oc1}) \end{aligned}$$

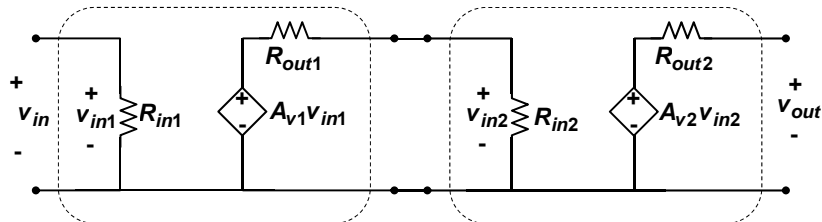
2)



Stage 2 Parameters:

$$\begin{aligned} R_{in2} &= \infty \\ R_{out2} &= (r_{o2} \parallel r_{oc2}) \\ A_{v2} &= -g_{m2}(r_{o2} \parallel r_{oc2}) \end{aligned}$$

## A Cascade of Two Amplifiers

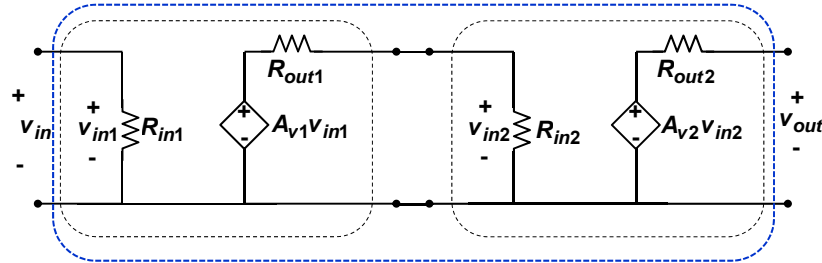


Open circuit voltage gain:

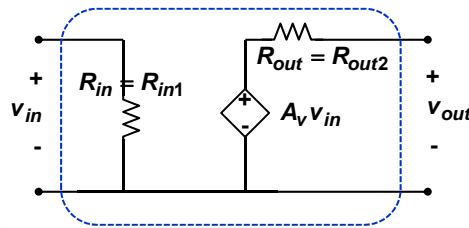
$$\begin{aligned} v_{out} &= A_{v2} v_{in2} = A_{v2} A_{v1} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \\ &= A_{v2} A_{v1} v_{in} \frac{R_{in2}}{R_{out1} + R_{in2}} \\ \Rightarrow A_v &= \frac{v_{out}}{v_{in}} = A_{v2} A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} \end{aligned}$$

Inter-stage voltage divider

### A Cascade of Two Amplifiers



The two stages can be combined into an equivalent single stage model:

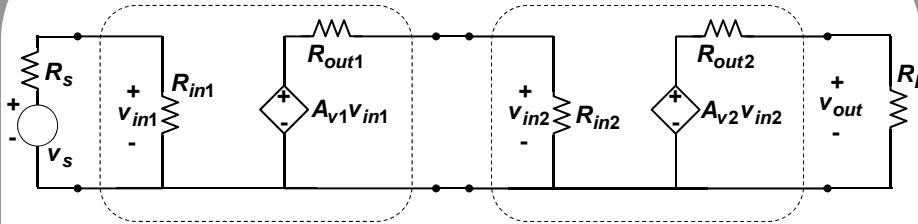


Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = A_{v2} A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}}$$

Inter-stage voltage divider

### A Cascade of Two Amplifiers with a Source Resistor



Voltage gain:

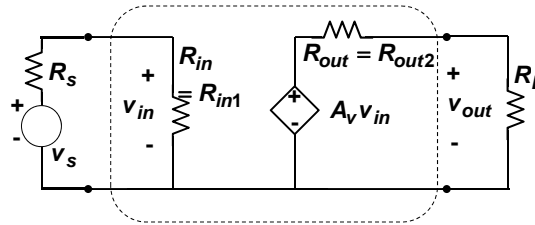
$$\begin{aligned} v_{out} &= A_{v2} v_{in2} \frac{R_L}{R_{out2} + R_L} = A_{v2} A_{v1} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \\ &= A_{v2} A_{v1} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \\ &= A_{v2} A_{v1} v_s \frac{R_{in1}}{R_s + R_{in1}} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \end{aligned}$$

For the CS FET stages:  
 $R_{in1} = R_{in2} = \infty$

$$\Rightarrow \frac{v_{out}}{v_s} = A_{v2} A_{v1} \frac{R_{in1}}{R_s + R_{in1}} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L}$$

Input voltage divider      Inter-stage voltage divider      Output voltage divider

### A Cascade of Two Amplifiers with a Source Resistor



One can also use the equivalent single stage mode to find the voltage gain:

$$\begin{aligned}
 v_{out} &= A_v v_{in} \frac{R_L}{R_{out2} + R_L} \\
 &= A_v v_s \frac{R_{in1}}{R_s + R_{in1}} \frac{R_L}{R_{out2} + R_L} \\
 \Rightarrow \frac{v_{out}}{v_s} &= A_v \frac{R_{in1}}{R_s + R_{in1}} \frac{R_L}{R_{out2} + R_L}
 \end{aligned}$$

Input voltage divider

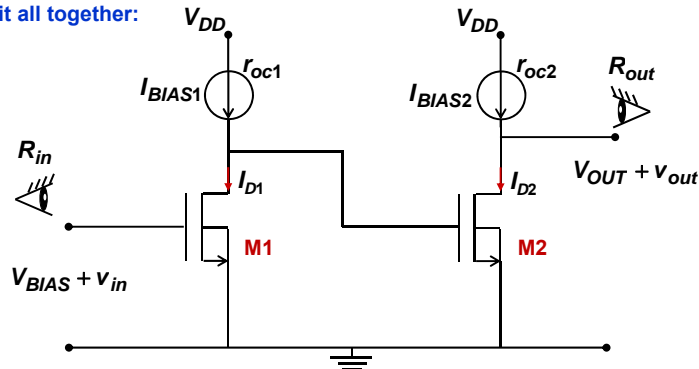
Output voltage divider

It is easier to use the single-stage model

The final expression is the same as the one on the previous slide

### A Cascade of Two CS Stages for a Voltage Amplifier

Putting it all together:



Input resistance:

$$R_{in} = \infty$$

Output resistance:

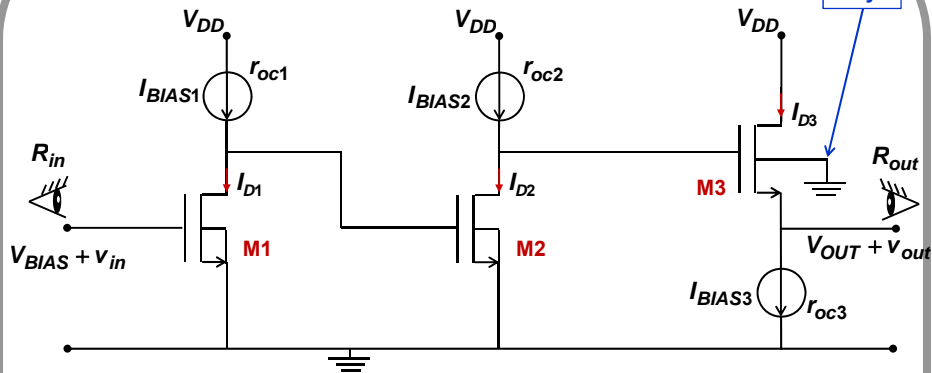
$$R_{out} = r_{o2} \parallel r_{oc2}$$

Open circuit voltage gain:

$$\begin{aligned}
 A_v = \frac{v_{out}}{v_{in}} &= A_{v1} A_{v2} \frac{R_{in2}}{R_{out1} + R_{in2}} \\
 &= [-g_{m1}(r_{o1} \parallel r_{oc1})] [-g_{m2}(r_{o2} \parallel r_{oc2})]
 \end{aligned}$$

Not really a good voltage amplifier – output resistance is too large – but a decent transconductance amplifier

### A Cascade of Three FET Stages: 2 CS and 1 CD



Input resistance:

$$R_{in} = \infty$$

Output resistance:

$$\frac{1}{R_{out}} \approx \frac{1}{r_{oc3}} + (g_{m3} + g_{mb3}) \approx (g_{m3} + g_{mb3})$$

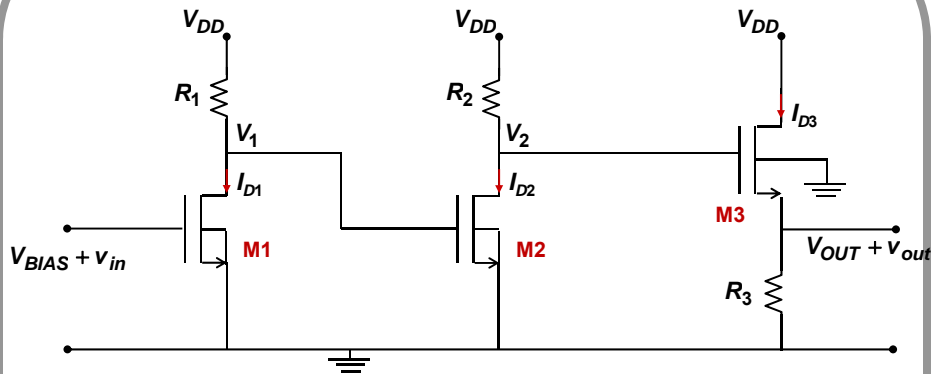
**Small**

Open circuit voltage gain:

$$A_v = A_{v1} A_{v2} A_{v3} \approx [-g_{m1}(r_{o1} \parallel r_{oc1})][-g_{m2}(r_{o2} \parallel r_{oc2})][\sim 1]$$

Now it is a better voltage amplifier!

### A Cascade of Three FET Stages: DC Biasing

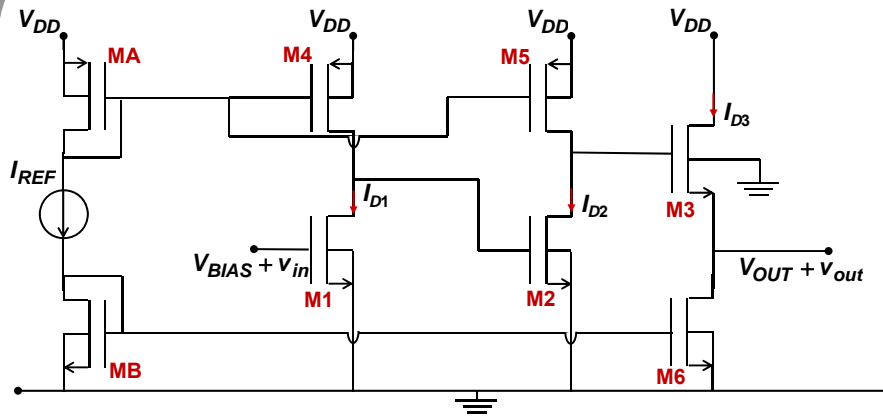


In the above scheme, the DC bias of one stage affects the DC bias of another stage

Need to ensure appropriate DC bias of every stage such that:

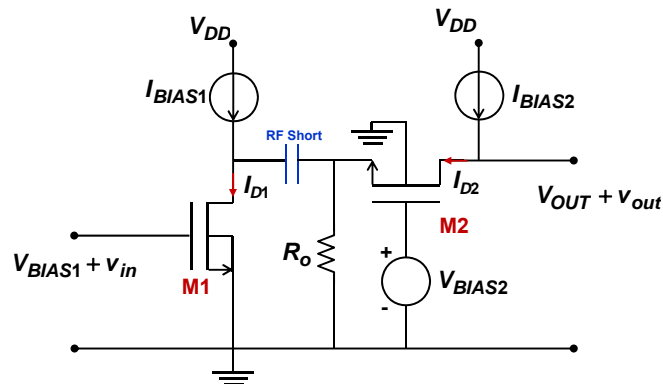
- i) The FETs are operating in saturation
- ii) The desired voltage swing does not cause problems (e.g. cause some FET to go out of saturation)

### A Cascade of Three FET Stages: Current Source Biasing



The sizes ( $W/L$  ratios) of **M4**, **M5**, and **M6** can be adjusted to get the desired bias currents for the three amplifier stages

### A Cascade of CS and CG: A Capacitively-Coupled Cascode



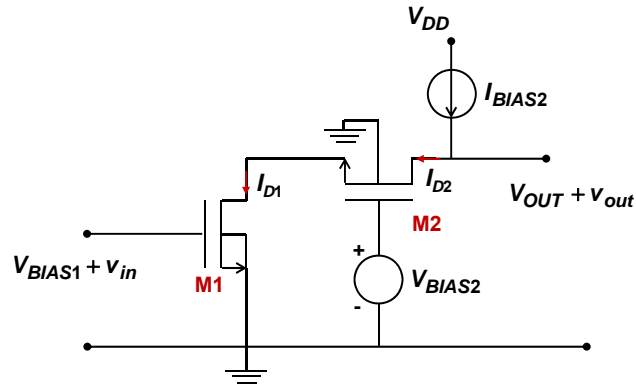
The FET cascode has a large input resistance, a very large output resistance, and a large gain

But it is much better than a CS-CS cascade in terms of the frequency performance, as we will see later in the course

The above topology can be simplified.....



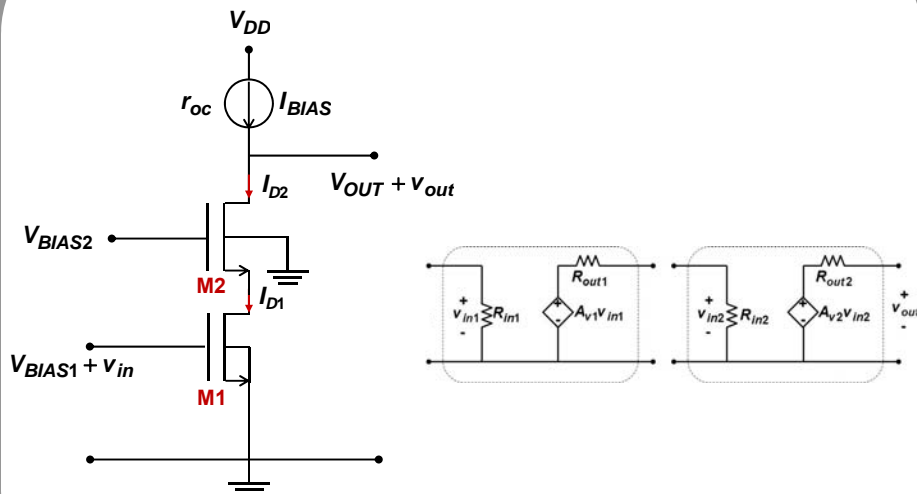
### A Cascade of CS and CG: A Direct-Coupled Cascode



One current source can bias both the stages in a direct-coupling topology....!

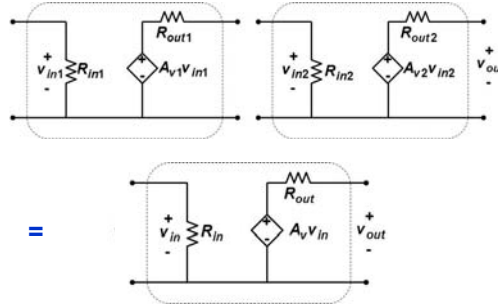
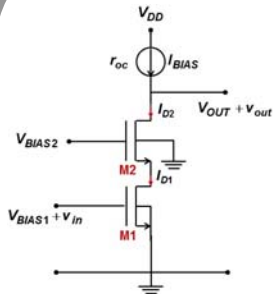
This is the preferred way for on-chip designs

### A Cascade of CS and CG: The Cascode



A different way to draw the same circuit

### The FET Cascode: Input and Output Resistances of Each Stage



Input resistances:

$$R_{in2} \approx \frac{1}{g_{m2} + g_{mb2}} \left( 1 + \frac{r_{oc}}{r_{o2}} \right)$$

Assuming  $R_L = \infty$

$$R_{in1} = \infty$$

$$\Rightarrow R_{in} = R_{in1} = \infty$$

Output resistances:

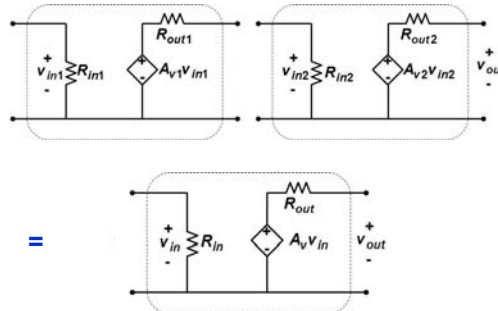
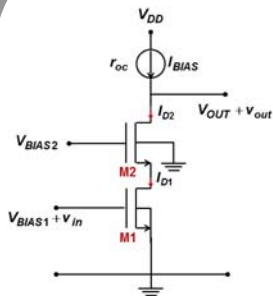
$$R_{out1} = r_{o1}$$

$$R_{out2} = r_{oc} \parallel [r_{o2} + R_{out1} + r_{o2}(g_{m2} + g_{mb2})R_{out1}]$$

$$\approx r_{oc} \parallel [(g_{m2} + g_{mb2})r_{o1}r_{o2}]$$

$$\Rightarrow R_{out} = R_{out2} \approx r_{oc} \parallel [(g_{m2} + g_{mb2})r_{o1}r_{o2}]$$

### The FET Cascode: Voltage Gains of Each Stage



Voltage Gains:

$$A_{v1} = -g_{m1}r_{o1}$$

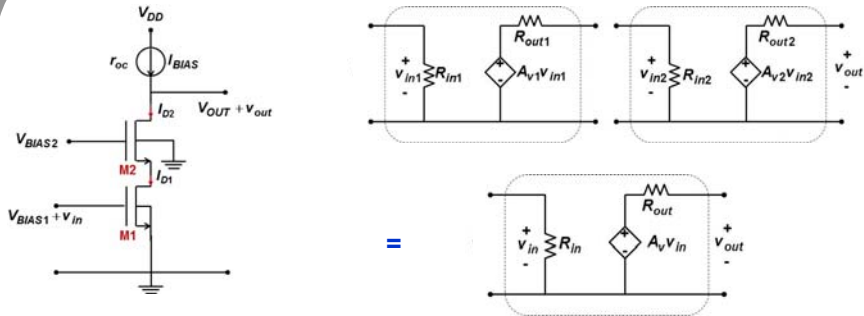
$$A_{v2} = \left( g_{m2} + g_{mb2} + \frac{1}{r_{o2}} \right) (r_{o2} \parallel r_{oc})$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} = (-g_{m1}r_{o1}) [(g_{m2} + g_{mb2})r_{o2} + 1] \frac{r_{oc}}{r_{o2} + r_{oc}} \frac{1}{(g_{m2} + g_{mb2})r_{o1} \frac{r_{o2}}{r_{o2} + r_{oc}} + 1}$$

If  $r_{oc} \gg r_{o2}, r_{o1}$ :

$$\Rightarrow A_v \approx [-g_{m1}r_{o1}] [(g_{m2} + g_{mb2})r_{o2} + 1] \approx [-g_{m1}r_{o1}] [(g_{m2} + g_{mb2})r_{o2}] \longrightarrow \text{Very large}$$

### The FET Cascode: Voltage Gains of Each Stage



Voltage Gains:

$$A_{v1} = -g_{m1}r_{o1} \quad A_{v2} = (g_{m2} + g_{mb2})(r_{o2} \parallel r_{oc})$$

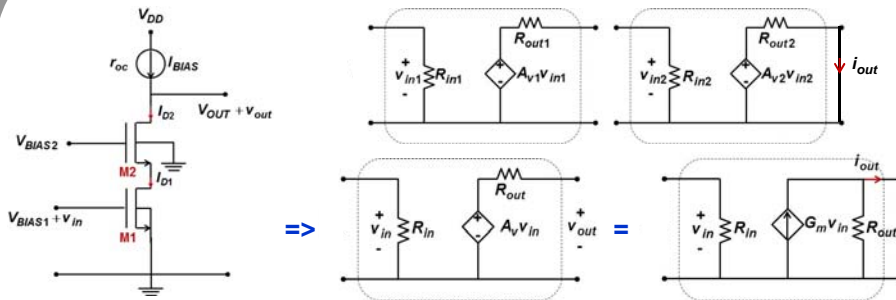
$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} = (-g_{m1}r_{o1}) \left( (g_{m2} + g_{mb2}) \frac{r_{o2}r_{oc}}{r_{o2} + r_{oc}} \right) \frac{1}{(g_{m2} + g_{mb2})r_{o1} \frac{r_{o2}}{r_{o2} + r_{oc}} + 1}$$

If  $r_{oc} \sim r_{o2}, r_{o1}$ :

$$\Rightarrow A_v \approx (-g_{m1}r_{o1}) \left( (g_{m2} + g_{mb2}) \frac{r_{o2}r_{oc}}{r_{o2} + r_{oc}} \right) \frac{1}{(g_{m2} + g_{mb2})r_{o1} \frac{r_{o2}}{r_{o2} + r_{oc}}}$$

$$\Rightarrow A_v \approx -g_{m1}r_{oc} \quad \longrightarrow \quad \text{Can still be large}$$

### The FET Cascode: Transconductance Gain



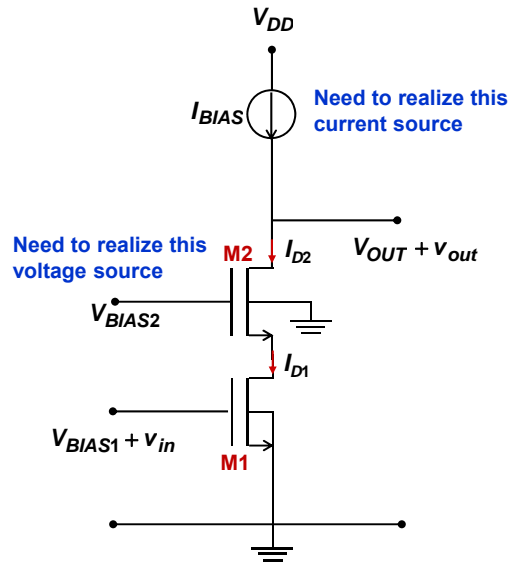
Transconductance Gain (with output shorted):

$$G_m = \frac{i_{out}}{v_{in}} = \frac{A_v}{R_{out}} \approx -g_{m1}$$

### Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

$$I_{D1} = I_{D2} = I_{BIAS}$$



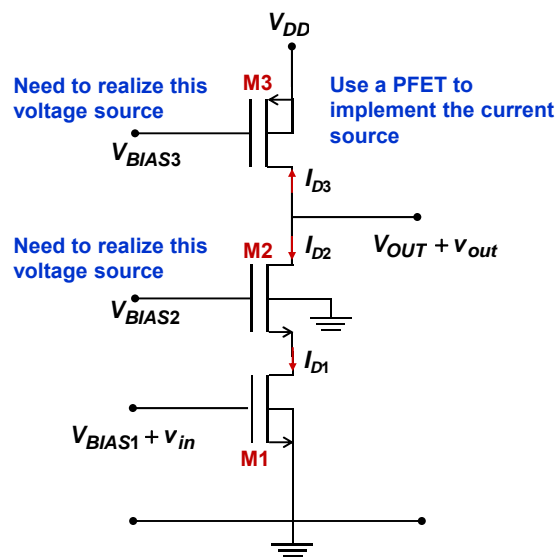
### Biasing the FET Cascode Amplifier

Choose voltage biasing such that:

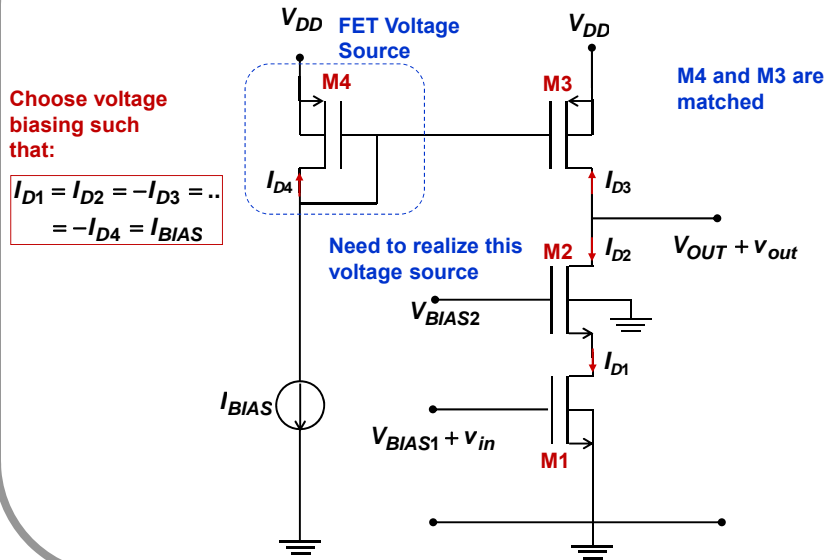
$$I_{D1} = I_{D2} = -I_{D3}$$

**Problem:** To be accurate with voltage biasing, one needs to know the characteristics (i.e.  $k_n$ ,  $k_p$ , etc) of the FETs accurately, and this information is usually not available to the circuit designer

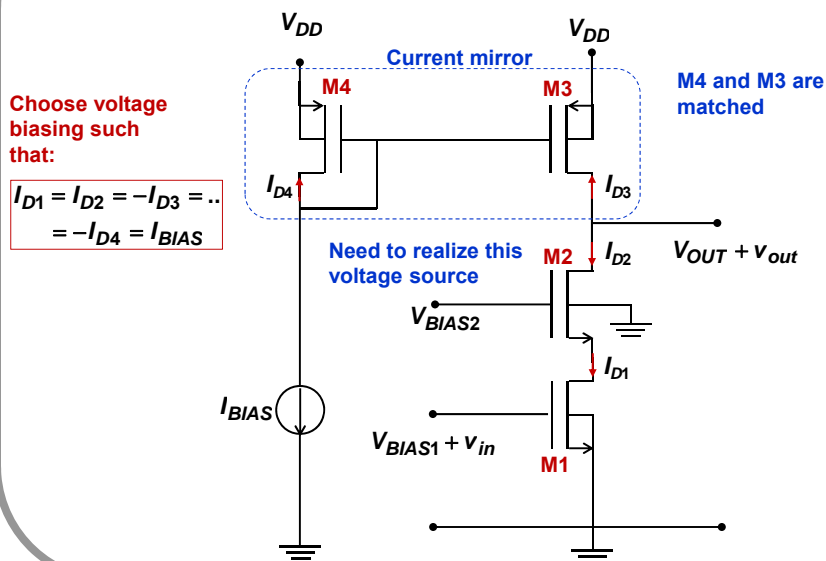
**Solution:** Use circuit biasing schemes that are not too sensitive to the circuit designer's detailed knowledge of the FETs!



### Biasing the FET Cascode Amplifier



### Biasing the FET Cascode Amplifier

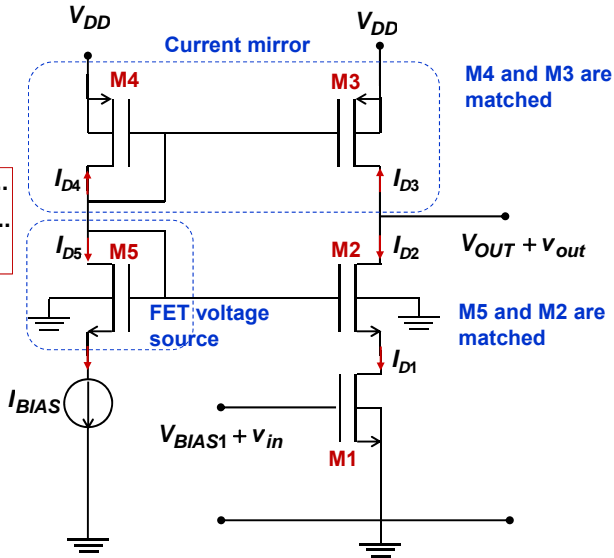


### Biasing the FET Cascode Amplifier

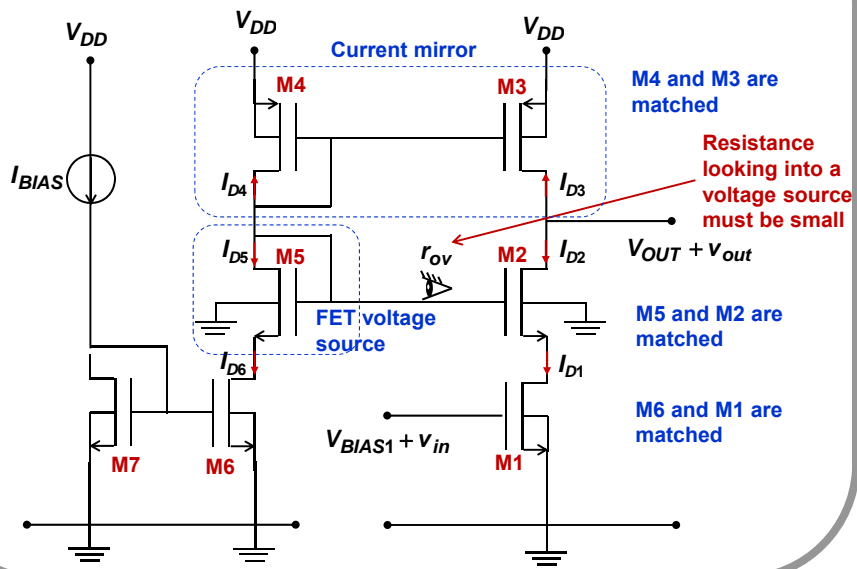
Choose voltage biasing such that:

$$\begin{aligned} I_{D1} &= I_{D2} = -I_{D3} = \dots \\ &= -I_{D4} = I_{D5} = \dots \\ &= I_{BIAS} \end{aligned}$$

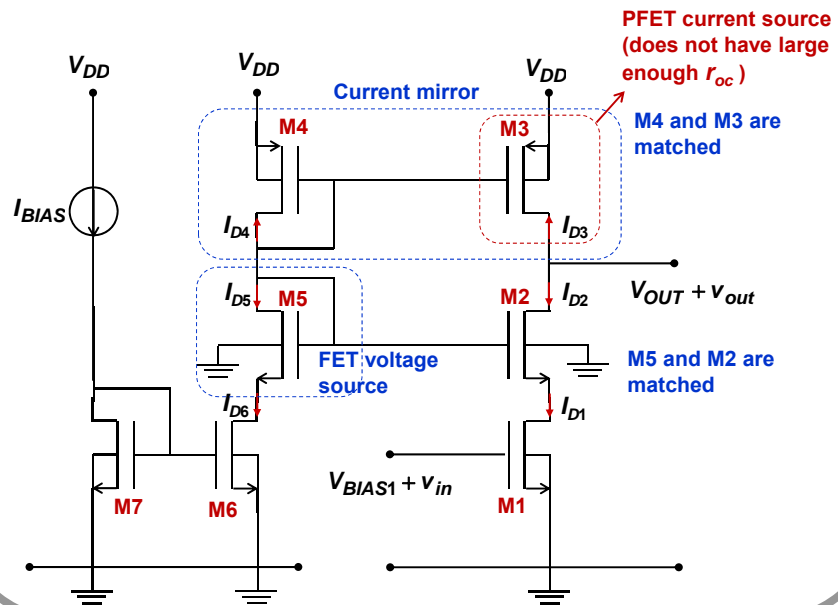
What if we have only a single stable current source available on the chip..?



### Biasing the FET Cascode Amplifier



### Biasing the FET Cascode Amplifier



### Improved FET Cascode Amplifier

