In this lecture you will learn:
- Current and voltage sources using FETs
- FET current mirrors
- Cascode current mirror
- Double Wilson current mirror
- Active biasing schemes

Motivation

**Questions:**
- Are there better ways to realize on-chip current sources to bias circuits?
- Are there good ways to generate on-chip voltage levels to bias circuits?

Using large resistors too often is not a good idea in integrated chips
### Characteristics of Ideal Current Sources and Sinks

**Ideal Current Sources:**

- One can have any voltage at the output terminals of an ideal current source and the current delivered will remain constant.
- The output resistance of an ideal current source is infinity.

**Ideal Current Sinks:**

- One can have any voltage at the output terminals of an ideal current sink and the current sunk will remain constant.
- The output resistance of an ideal current sink is infinity.

### Characteristics of Ideal Voltage Sources

**Ideal Voltage Sources:**

- One can draw any current from an ideal voltage source and the voltage at the output terminals will remain constant.
- The output resistance of an ideal voltage source is zero.

**Non-Ideal Voltage Sources:**

- The output resistance of a non-ideal voltage source is not zero.
- The slope is given by \( \frac{1}{r_{ov}} \).
A FET Voltage Source: Large Signal Analysis

- Assume for the moment that we have a current source $I_{REF}$

$$I_{REF} = I_D + I_{OUT} = \frac{k_n}{2} (V_{OUT} - V_{TN})^2 (1 + \lambda_n V_{OUT}) + I_{OUT}$$

$$\Rightarrow V_{OUT} \approx V_{TN} + \sqrt{\frac{2(l_{REF} - l_{OUT})}{k_n}}$$

(if $\lambda_n V_{OUT} \ll 1$)

- The line can be made more vertical and the voltage source more ideal by increasing the value of $g_m$.

Non-Ideal Voltage Source

- Slope

$$\frac{dl_{OUT}}{dV_{OUT}} = -g_m = -k_n (V_{OUT} - V_{TN})$$

Increasing ($W/L$)

- If the $(W/L)$ ratio of the FET is made very large, the output voltage $V_{OUT}$ is fixed at approximately $V_{TN}$ for all values of the current $I_{OUT}$ drawn from the source (provided $I_{OUT} < I_{REF}$).
A FET Voltage Source: Small Signal Analysis

Need to find the resistance $r_{ov}$ looking into from the output terminals.

Small signal model:

$V_{DD}$

$V_{OUT}$

$I_{REF}$

$I_{OUT}$

$r_{ov}$

$V_{DD}$

Small signal

$I_{REF}$

$I_{OUT}$

$r_{ov}$

Need to find the resistance $r_{ov}$ looking into from the output terminals.

Small signal model:

$V_{DD}$

$V_{OUT}$

$I_{REF}$

$I_{OUT}$

$r_{ov}$

$V_{DD}$

Small signal

$I_{REF}$

$I_{OUT}$

$r_{ov}$

Need to find the resistance $r_{ov}$ looking into from the output terminals.
A FET Voltage Source: Small Signal Analysis

Small signal resistance looking into the voltage source is:

\[ r_{ov} = \left( \frac{1}{g_m} \right) || r_o || r_{oc} = \frac{1}{g_m} \]

Generally small if \( g_m \) is large

We have a voltage source that:

- Gives a DC voltage \( V_{OUT} \) adjustable by changing the value of \( I_{REF} \), and
- Has an incremental or small signal resistance \( r_{ov} \) approximately equal to \( 1/g_m \) (which can be pretty small)

A FET Voltage Source: Simplest Implementation of \( I_{REF} \)

If \( V_{OUT} > V_{TN} \):

\[
\frac{V_{DD} - V_{OUT}}{R} = I_D + I_{OUT} = \frac{k_n (V_{OUT} - V_{TN})^2}{2} + I_{OUT}
\]

\[
\Rightarrow V_{OUT} = V_{TN} + \frac{1}{k_n R^2} + \frac{2(V_{DD} - V_{TN}) R - I_{OUT}}{k_n} - \frac{1}{k_n R}
\]

Slope when \( R \) is much larger than \( 1/g_m \)

\[
\frac{dI_{OUT}}{dV_{OUT}} = -g_m = -k_n (V_{OUT} - V_{TN})
\]

* If the \((W/L)\) ratio of the FET is made very large and \( R \) is much larger than \( 1/g_m \), the output voltage \( V_{OUT} \) is fixed at approximately \( V_{TN} \) for all values of the current \( I_{OUT} \) drawn from the source - provided \( I_{OUT} < (V_{DD} - V_{TN})/R \)
FET Voltage Sources

One can produce multiple voltage levels from the same structure using NMOS FETs, PMOS FETs, and combination of both NMOS and PMOS FETs.

\[ V_1 = V_2 + V_{TN1} + \frac{2(l_{REF} - I_1)}{k_{n1}} \]
\[ V_2 = V_{TN2} + \frac{2(l_{REF} - I_1 - I_2)}{k_{n2}} \]

But ………need to be careful about the small signal resistances associated with each voltage output!

FET Voltage Sources: Small Signal Analysis

Find the resistance looking into the first voltage source assuming the second one is incrementally open (why?)
FET Voltage Sources: Small Signal Analysis

Find the resistance looking into the first voltage source assuming the second one is incrementally open (why?)

\[ r_{ov1} \approx \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \rightarrow \text{Small} \]
FET Voltage Sources: Small Signal Analysis

Then find the resistance looking into the second voltage source assuming the first one is incrementally open (why?)

\[ r_{ov2} \approx \frac{1}{g_{m2}} \rightarrow \text{Small} \]

A FET Current Sink: Large Signal Analysis

• Assume that we have a single current source \( I_{REF} \) - but we want more……

In saturation:

\[ I_D = \frac{k_p}{2} (V_{GS} - V_{TN})^2 (1 + \lambda_n V_{DS}) \]

\[ k_p = \frac{W}{L} \mu_n C_{ox} \]

\[ \lambda_n \] Small

Assuming \( M_2 \) is in saturation

\[ V_{GS1} = V_{GS2} \]

\[ \Rightarrow I_{D2} = \frac{k_{n2}}{k_{n1}} I_{D1} = \left( \frac{W/L}{W/L} \right) I_{D1} \]

\[ \Rightarrow I_{OUT} \approx \left( \frac{W/L}{W/L} \right) I_{REF} \]

\[ \frac{dI_{OUT}}{dV_{OUT}} = \frac{1}{r_{o2}} \]

• Not exactly the horizontal line of an ideal current source but good enough for many practical applications
A FET Current Mirror

- A ideal current mirror duplicates the current:
  \[ I_{OUT} = I_{REF} \]

\[ V_{GS2} = V_{GS1} \]
\[ (W/L)_2 = (W/L)_1 \]
\Rightarrow \[ I_{OUT} = I_{REF} \]

\[ \text{Matched Transistors} \]

- A matched transistor pair

A FET Current Sink: Small Signal Analysis

\[ r_{oc} = r_{o2} = \frac{1}{g_{o2}} \]

- We have a current sink that:
  - Provides a DC current \( I_{OUT} \) adjustable by changing the value of \( I_{REF} \), and
  - Has an incremental or small signal resistance \( r_{oc} \) approximately equal to \( r_{o2} \) (which can be pretty large)
  - The resistance \( r_{oc} \) will become small if M2 goes into the linear region
One can realize multiple current sinks for biasing applications from the same structure using NMOS devices with different \((W/L)\) ratios:

\[
I_{Dk} = \frac{(W/L)_k}{(W/L)_1} I_{REF}
\]

Note that \(V_{OUTk}\) needs to be always large enough such that \(M_k\) remains in saturation.

A PFET Current Source and Current Mirror

- A current mirror duplicates the current: \(I_{OUT} = I_{REF}\)

\[
\begin{align*}
V_{GS2} &= V_{GS1} \\
(W/L)_2 &= (W/L)_1 \\
\Rightarrow I_{OUT} &= I_{REF}
\end{align*}
\]

Matched Transistors

A matched transistor pair
One can realize multiple current sources for biasing applications from the same structure using PMOS devices with different \( \frac{W}{L} \) ratios:

\[
I_{OUTk} = \frac{(W/L)_k}{(W/L)_1} I_{REF}
\]

Note that \( V_{OUTk} \) needs to be always small enough such that \( M_k \) remains in saturation.

\[r_{oc} = r_{o2} = \frac{1}{g_{o2}}\]

\[r_{oc} = r_{o3} + r_{o4}(1+g_{m3}r_{o3}) = g_{m3}r_{o3}r_{o4}\]
A Current Sink with Large Output Resistance: The Cascode Design

Usually the substrate contact of all NFETs in the stack are tied to the ground in CMOS technologies in which all NFETs share the same substrate.

Need to account for the body effect (due to non-zero $V_{SB}$) in M3.

The Double Wilson Current Mirror

More immune to systemic errors in the fabrication process than the cascode design.
A PFET Current Source: The Cascode Design

Usually the substrate contact of all PFETs in the stack are tied to $V_{DD}$ in CMOS technologies in which all PFETs share the same substrate.

Need to account for the body effect (due to non-zero $V_{SB}$) in M3.
Biasing the PFET Loaded NFET CS Amplifier

If M4 and M5 are identical and M3 and M6 are identical (matched pairs) then \( I_D \) will equal \( I_{REF} \) and the gate voltages needed for M5 and M6 will be automatically generated on the chip without exact knowledge of the \( k_p \) and \( V_{TP} \) of the PFETs.

Voltage biasing network:

- Voltage biasing network
- Matched pairs
- PFET cascode load
Biasing the PFET Loaded NFET CS Amplifier

The diagram illustrates a circuit with matched pairs of transistors, labeled M1 to M7. The circuit includes a biasing current source labeled $I_{REF}$ and a voltage source $V_{DD}$. The load is represented by a cascode configuration with transistors M5 and M6. The output is denoted as $V_{OUT} + v_{out}$ and $V_{OUT} - v_{out}$.

The circuit is designed to provide a high impedance output and can be used in applications requiring a cascode current amplifier.
So we implemented a current source load using the PFETs in a cascode configuration.