11.1)

a) The circuit, as redrawn above, is a just a PFET Clapp oscillator.

b) Proper DC biasing is critical to the operation of this circuit. The DC current through the drain of the PFET and through the resistor/inductor paths add together and equal the current \( I_{BIAS} \) pulled down by the current source. Therefore,

\[
I_{BIAS} = \frac{k_p}{2} (V_{IN} - V_{DD} - V_{TP})^2 + \frac{V_{DD} - V_{IN}}{R}
\]

At DC,

\[
V_D = V_{IN} \\
V_{DS} = V_D - V_{DD} = V_{GS} = V_{IN} - V_{DD}
\]

Therefore, the PFET will either be in saturation or cut-off (it is diode-connected at DC when the inductor is a short). For the PFET to be in cut-off, \( I_D = 0 \), and,

\[
V_{GS} > V_{TP} \\
\Rightarrow V_{IN} - V_{DD} > V_{TP} \\
\Rightarrow \frac{V_{DD} - V_{IN}}{R} < -\frac{V_{TP}}{R}
\]

\[
\Rightarrow I_{BIAS} < -\frac{V_{TP}}{R}
\]

c) First draw the full small signal model:

You can ignore \( r_o \) as the problem suggests. The doing KCL at node (1) gives,
\[
\frac{v_{in}}{R + j\omega C_1 + \frac{1}{j\omega L}} = \frac{v_d}{j\omega L}
\]

And KCL at the drain gives,
\[
v_d \left( j\omega C_2 + \frac{1}{j\omega L} \right) = v_{in} \left( \frac{1}{j\omega L} - g_m \right)
\]

Combining these two equations gives,
\[
\left[-\omega^2 L \left( C_1 + C_2 \right) + \omega^4 L^2 C_1 C_2 + \frac{j\omega L}{R} \left( 1 - \omega^2 L C_2 + g_m R \right) \right] v_{in} (\omega) = 0
\]

d) The real and imaginary parts of the expression in the square brackets must separately equal to zero. Setting the real part to zero gives the oscillation frequency,
\[
\omega = \sqrt{\frac{\left( C_1 + C_2 \right)}{C_1 C_2 L}}
\]

e) Setting the imaginary part to zero (and using the result from part (d)) gives the oscillation condition,
\[
g_m R \frac{C_1}{C_2} = 1
\]

The above value of \( g_m \) is the minimum value of \( g_m \) needed for oscillation.

f) Suppose the circuit was oscillating in steady state, with a small signal amplitude, and with a value of \( g_m \) that satisfied the condition in part (e). Suppose the value of \( g_m \) was then suddenly increased (by, say, increasing the bias current value). Now the value of \( g_m \) is larger than the minimum value indicated in part (e) above and this means that the circuit has more SMALL SIGNAL gain than needed to meet the gain=loss condition. In other words, the net loop gain is greater than unity. Therefore, the oscillating signal would start to amplify and keep getting larger. As the signal amplitude gets larger (and possibly goes outside the small signal range of operation), gain saturation would set in. This gain saturation would then reduce the average gain (or average \( g_m \)) experienced by the signal until the loop gain is back to unity and a steady state oscillation is achieved but now at a larger oscillating signal amplitude than the amplitude before the value of \( g_m \) was increased.

11.2)
a) The base-emitter PN junction in a BJT is usually current biased. A standard way of achieving this is to use a resistor in series with a voltage source in series with the PN junction, rather than directly hooking the PN junction to a voltage source. The resistor $R_1$ is effectively current biasing the base-emitter PN junction.

\[ I_B = \frac{I_C}{\beta_F} = 10 \mu A \text{ and,} \]
\[ V_{OUT} = V_{DD} - I_C R = 2.5 \text{ V} \]
\[ \Rightarrow R = \frac{V_{DD} - 2.5}{I_C} = 2.5 \text{ k}\Omega \]

\[ \left| V_{OUT} \right|_{\text{max}} = V_{DD} = 5 \text{ V} \]
\[ \left| V_{OUT} \right|_{\text{min}} = V_{CE-SAT} = 0.2 \text{ V} \]

\[ V_{DD} - \beta_F I_B \left|_{\text{max}} \right. = V_{CE-SAT} = 0.2 \text{ V} \]
\[ \Rightarrow I_B \left|_{\text{max}} \right. = 19.2 \mu A \]
\[ \text{and,} \]
\[ I_B \left|_{\text{min}} \right. > 0 \]

\[ V_{DD} = I_B R_1 + V_{BE-ON} = I_B R_1 + 0.6 \]
\[ \Rightarrow R_1 = 229 \text{ k}\Omega \]
\[ i_c = g_m v_\pi + \frac{v_{out}}{r_o} \]

\[ v_{out} = -i_c R \]

\[ \Rightarrow v_{out} = -g_m (r_o \parallel R) v_\pi \]

\[ \Rightarrow A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \parallel R) \]

g)

\[ v_{in} = v_s \frac{(r_\pi \parallel R_1)}{(r_\pi \parallel R_1) + R_s} \]

Therefore,

\[ A_v = \frac{v_{out}}{v_{in}} \frac{v_{in}}{v_s} = -g_m (r_o \parallel R) \frac{(r_\pi \parallel R_1)}{(r_\pi \parallel R_1) + R_s} \]

If the resistor \( R_1 \) is too small then it will effectively short the input signal, thereby reducing the total gain.

h)

\[ g_m = \frac{qI_C}{KT} \]

\[ g_o = \frac{1}{r_o} = \frac{I_C}{V_A} \]

\[ A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \parallel R) = -92 \]

i) Note that:

\[ V_{OUT} = V_{DD} - I_C R = 2.5 \text{ V} \]

\[ \Rightarrow I_C R = 2.5 \text{ V} \]

And, \( A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \parallel R) \approx -g_m R = -\frac{q(I_C R)}{KT} \). So the gain largely depends on the value of the product \( I_C R \) which is fixed by \( V_{OUT} \). So gain cannot be changed much if \( V_{OUT} \) is fixed.