Problem 10.1: (Frequency performance of a cascode amplifier vs a common source amplifier)

Consider the following cascode amplifier:

- \( W = 10 \, \mu m \)
- \( L = 0.5 \, \mu m \)
- \( \mu_n C_{ox} = 200 \, \mu A/V^2 \)
- \( \lambda_n = 0.02 \, 1/V \)
- \( V_{DD} = 3.0 \, V \)
- \( V_{TN} = 0.5 \, V \)
- \( I_{BIAS} = 4 \, mA \)
- \( C_{gd} = 10 \, fF \)
- \( C_{gs} = \frac{2}{3} C_{ox}WL = 30 \, fF \)
- \( r_{oc} \approx r_{o2} = r_{o1} \)
Assume that $V_{BIAS1}$ and $V_{BIAS2}$ have been adjusted such that the drain current of the both the FETs is 4 mA. Suppose $R_s = 2k\Omega$.

**Synopsis:** A good voltage amplifiers needs to have a large input resistance, a small output resistance, a large gain, and a large gain bandwidth (i.e. the bandwidth over which the gain is flat and at the DC value is large).

A common source amplifier has a large gain and a large input resistance, but suffers from the Miller effect which compromises the gain bandwidth.

A common gate amplifier has a large gain, and a large gain bandwidth (because it does not suffer from the Miller effect), but it has a small input resistance.

A casacade of the above two, i.e. a cascode, has a large input resistance, a large gain, and a large gain bandwidth. The large gain bandwidth of the cascode results from the fact that the first common source stage in a cascode doesn’t really produce too much gain (because it gets loaded with the small input resistance of the second common gate stage) and most of the gain comes from the second common gate stage. Consequently, the Miller effect present in the first common source stage is not too damaging. These characteristics make the cascode an attractive stage for circuit designers. In this problem you will explore this in detail.

a) Draw a high-frequency small signal model of the cascode shown above.

b) At the bias point, find the (numerical) values of $g_m$ and $g_o$ for both the FETs (these should be identical for the two FETs since they are both biased with the same DC current). How big is $g_m$ compared to $g_o$?

c) Using KCL at the drain end of M2 in the small signal model, show that:

$$v_{out} \approx \frac{g_{m2}(r_{oc} \parallel r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \parallel r_{o2})}$$

The above expression is the open circuit voltage gain of the second common gate stage. At low frequencies (~DC), the above expression gives the familiar near-DC open circuit voltage gain of a common gate amplifier: $g_{m2}(r_{oc} \parallel r_{o2})$.

d) Plot $10\log_{10}\left(\frac{v_{out}}{v_{in}}\right)^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency in Hz (not rad/s). The matlab function “logspace” will be useful when making the frequency array for plotting.

e) Using KCL at the drain end of M1 in the small signal model, show that:

$$\frac{v_{in}}{v_{out}} \approx -\frac{g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{o2} + g_{m2} + j\omega(C_{gd1} + C_{gs2}) - g_{o2} \frac{g_{m2}(r_{oc} \parallel r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \parallel r_{o2})}}$$

If the input impedance looking into M2 from the source end were assumed to be infinite, the above expression would reduce to,
\[ v_a \approx -g_{m1} + j\omega C_{gd1} \]
\[ v_{in} \approx \frac{g_{m1} + j\omega C_{gd1}}{g_{m2} + j\omega (C_{gd1} + C_{gs2})} \]

which is the just the open circuit voltage gain of a common source amplifier with a low frequency value equal to \(-g_{m1}r_{o1}\). However, the input impedance of the common gate amplifier is not infinite and is in fact very small. After making suitable approximations, the above expression simplifies to,

\[ \frac{v_a}{v_{in}} \approx -g_{m1} + j\omega C_{gd1} \]
\[ \frac{g_{m2} + j\omega (C_{gd1} + C_{gs2}) - g_{o2}}{1 + j\omega C_{gd1}(r_{oc} || r_{o2})} \]

The near-DC value of the above expression is,

\[ \frac{v_a}{v_{in}} \approx -g_{m1}r_{o1} \]
\[ \frac{R_{out1} = r_{o1}}{R_{in2} \approx \frac{1}{g_{m2}(1 + \frac{r_{oc}}{r_{o2}})}} \]

\( v_a/v_{in} \) at near-DC is of the order of unity. What the above analysis shows is that the first stage, the common source stage, does not really provide much gain at all. All the gain comes from the second stage, the common gate stage. The first stage does not provide much gain because it is loaded with the small input resistance of the second stage. And so the loaded voltage gain of the first stage (not the open circuit voltage gain) is pretty small, near unity! Now here comes the punch line: since the first common source stage does not really provide much gain, the Miller effect does not make the gate-to-drain capacitance of the first stage look terribly big and therefore the Miller effect does not destroy the high frequency performance of the first common source stage!

f) Plot \(10\log_{10} \left| \frac{v_a}{v_{in}} \right|^2\) (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

g) Do a KCL at the gate of M1, used previously obtained results, and show that,

\[ \frac{V_{in}}{V_s} \approx \frac{1}{1 + j\omega (C_{gs1} + C_{gd1})(R_s - j\omega C_{gd1}R_s) - g_{m1} + j\omega C_{gd1}} \]
\[ \frac{g_{m2} + j\omega (C_{gd1} + C_{gs2}) - g_{o2}}{1 + j\omega C_{gd1}(r_{oc} || r_{o2})} \]

h) Plot \(10\log_{10} \left| \frac{v_{in}}{v_s} \right|^2\) (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

i) Based on the results in part (d) and (f) and (h), which stage, first or second or the input part, limits the overall frequency bandwidth of the amplifier?
j) Now using your results from parts (c), (e), and (g), Plot $10 \log_{10} \left( \frac{|v_{out}|}{|v_s|} \right)^2$ (i.e. in dB units) on a log-frequency scale from $1 \times 10^6$ Hz to $1 \times 10^{12}$ Hz. Note the 3dB corner frequency.

k) If you now just consider a simple common source amplifier (assume that the FET M2 is replaced by a wire) then from the lecture notes (without making approximations):

\[
\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{oc} + j\omega C_{gd1}}
\]
\[
\frac{v_{in}}{v_s} \approx \frac{1}{1 + j\omega(C_{gs1} + C_{gd1})R_s - j\omega C_{gd1}R_s \left[ \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{oc} + j\omega C_{gd1}} \right]}
\]

Plot $10 \log_{10} \left( \frac{|v_a|}{|v_s|} \right)^2$ (i.e. in dB units) on a log-frequency scale from $1 \times 10^6$ Hz to $1 \times 10^{12}$ Hz. Note the 3dB corner frequency. Compare the plot to your answer in part (j) for the cascode amplifier. You should see that the cascode does better in terms of the frequency bandwidth while providing at the same time few dB larger near-DC gain.

l) There is still a problem with using the cascode as a voltage amplifier; it has a large output resistance. This can be fixed by using a common drain stage as the final output stage. Do you think that adding a common drain stage would significantly spoil the frequency performance of the overall amplifier? Why or why not? Does a common drain stage suffer from the Miller effect?

**Problem 10.2: (RF Amplifier/Filter in one)**

Many CMOS RF receiving modules in wireless systems use a RF band-pass filter and an amplifier combination before demodulating or mixing down the RF signal. Often the filtration and amplification processes can be combined in a single stage. One such CMOS stage is shown in the figure below and has been implemented in the 100 nm CMOS technology. The “100 nm” refers to the FET channel length. In its simplest form, the CS stage is loaded with a LC circuit. Placing an inductor in a CMOS chip is not an easy task but can be done. The figure below also shows the micrograph of a CMOS GSM receiver chip with two integrated spiral inductors.

You will need to figure out the frequency response of the circuit. The operation of the circuit is as follows: We know that the resistance of the load sitting on top of the FET determines the gain of a CS stage. If a simple resistor is replaced by an LC circuit then the impedance of the LC circuit will be frequency dependent and therefore the CS stage gain can also be made frequency dependent. At low frequencies we expect the inductor to act like a short and therefore the amplifier gain will be very small. At high frequencies we expect the capacitor to act like a short and therefore the gain will again be very small. At some intermediate frequency the gain will be maximum and this maximum gain will occur in a very narrow band of frequencies. One can choose values for $L$ and $C$ so that the maximum gain occurs at around $\sim 1$ GHz (which is close to the carrier frequency used by mobile systems, e.g. GSM).
Suppose:

\[ \frac{W}{L} = 8 \quad C_{gs} = 0.5 \text{ fF} \quad C_{gd} = 0.1 \text{ fF} \]
\[ \mu_n C_{ox} = 200 \mu \text{A/V}^2 \quad R_s = 10 \text{ k}\Omega \]
\[ \lambda_n = 0.04 \text{ V} \quad L = 25 \text{ nH} \quad C = ? \text{ pF} \]
\[ V_{DD} = 3.5 \quad V_{BIAS} = 2.5 \quad V_{TN} = 0.5 \text{ V} \]

a) What ought to be the value of the capacitor \( C \) so that the maximum gain occurs at \( \sim 1 \text{ GHz} \)?

b) What is the impedance \( Z(\omega) \) of the load sitting on top of the FET?

c) Draw a small signal model of the circuit. Use the high frequency small signal model for the FET. Represent the LC load by its impedance \( Z(\omega) \).

d) Find the small signal voltage gain of the amplifier:

\[ A_v(\omega) = \frac{v_{out}(\omega)}{v_s(\omega)} \]

The best way to do it is to first find:

\[ \frac{v_{out}}{v_{in}} \]

and then find:

\[ \frac{v_{in}}{v_s} \]

and then multiply the two.

e) Plot the gain (in dB units: i.e. \( 20 \log_{10}|A_v| \) ) as a function of frequency from 10 MHz to 100 GHz. Use matlab or your favorite plotting program.

f) What is the maximum gain (in dB units) you see in your plot in part (e)?

g) What is the full width half max (FWHM) gain bandwidth you see in your plot in part (e)? FWHM gain bandwidth is the range of frequencies (in Hz) over which the gain (in dB) is larger than the peak gain value (in dB) minus 3 dB. In other words, FWHM gain bandwidth is the range of frequencies over which the square magnitude of the gain is more than one-half of the peak gain value.
h) Derive an analytic expression for the FWHM gain bandwidth and show that it matches what you see in your plot. Hint: using open circuit time constant technique determine the effective resistance associated with the LC circuit.

i) A simple inductor loaded CS stage can also perform well at high frequencies compared to a resistively loaded CS stage in terms of gain and output voltage swing. Suppose in the problem, the LC circuit is replaced by just an inductor of inductance 25 nH. Find the small signal voltage gain of the amplifier:

\[ A_v(\omega) = \frac{v_{\text{out}}(\omega)}{v_s(\omega)} \]

Plot the gain (in dB units: i.e. \(20 \log_{10}|A_v|\)) as a function of frequency from 10 MHz to 100 GHz. Use matlab or your favorite plotting program. You will note that there is no bandpass filtering but the gain still peaks around 15-16 GHz and is pretty large. You could not have easily obtained such a large gain at such high frequencies using a standard resistive load.

### Problem 10.3: (Folded Cascode Differential Amplifier)

Consider the following folded cascode differential amplifier. Use the low-frequency circuit models for this problem.

The FETs M1 and M2, M3 and M4, and M5 and M6 are matched pairs. The output resistances of sources \(I_{\text{BIAS}}\) are assumed to be infinity (for convenience). Assume appropriate DC biasing such that the currents in the two legs of the first stage are identical, and the currents in the two legs of the second stage are also identical.

- a) Find the differential mode gain \(A_{\text{vd}}\) of the amplifier assuming a differential small signal input.
- b) Find the short circuit output current (i.e. current flowing in the output when the output is shorted to the ground) assuming a differential small signal input.
- c) Find the output resistance of the amplifier.